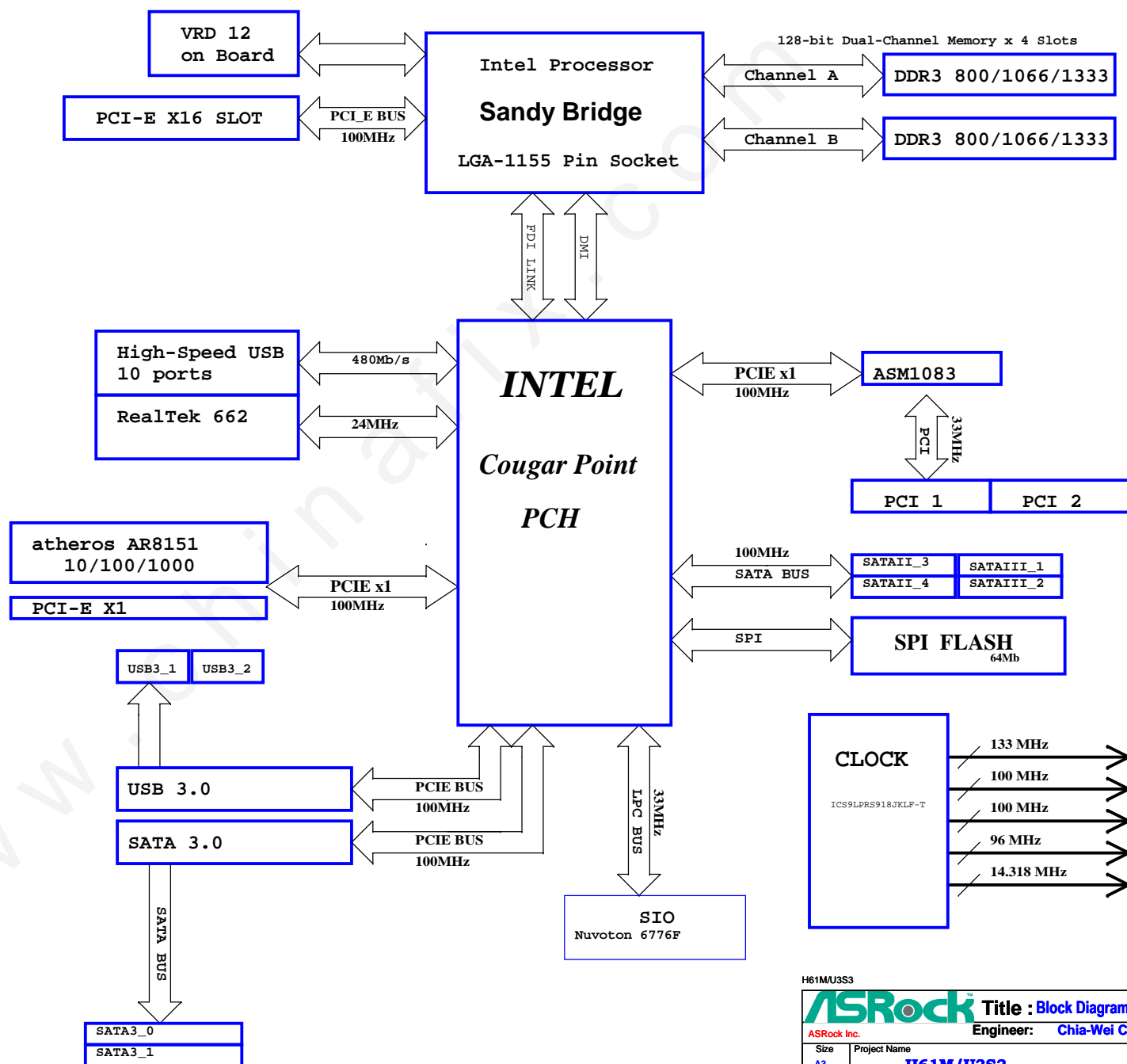


H61M/U3S3

Revision: R1.02

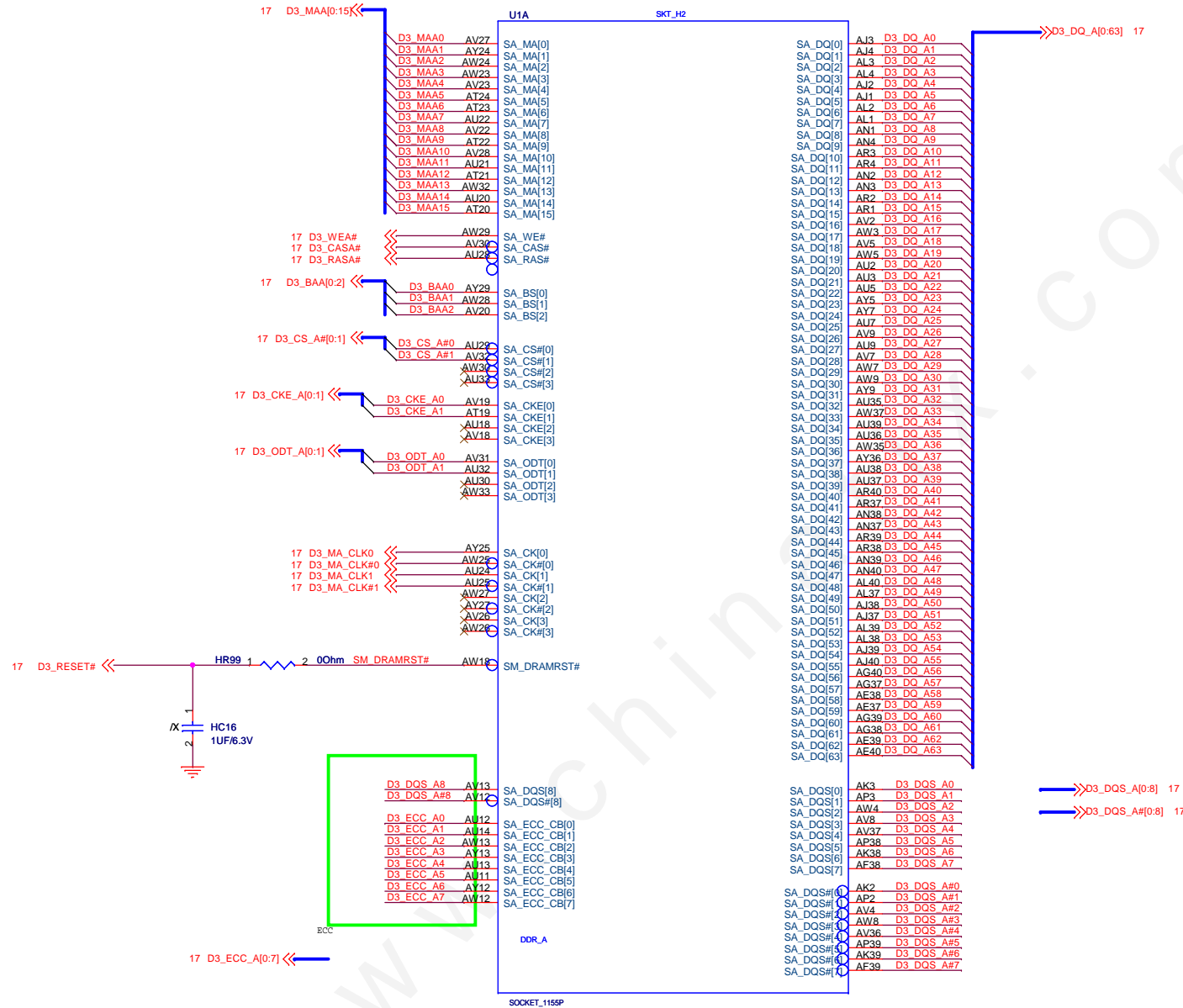
Block Diagram

PAGE	TITLE
01	History & Block
02~07	CPU: SOCKET 1155
08~16	INTEL PCH - Cougar Point
17	DDR3 CHANNEL A & B
18	DDR3 CHANNEL POWER
19	PCI-E X1 & X16
20	SATA2
21	LAN AR8151
22	USB Port & KB
23	PCI Solt
24~25	ALC 662
26	SIO 6776F
27	ASM 1083
28	POK & DualSW
29	IO CONNECTOR
30	VGA CON.
31	DVI CON.
32	HDMI CON.
33	SMBUS & ESD
34	Vcore - RT8859M
35	Vcore - CAP & Droop
36	OTP
37	VCCM Power
38	VTT Power
39	VCCSA Power
40	DC to DC POWER
41	USB3 IC & Con.
42	SATA3 IC & Con.
43	USB3 & SATA3 Power
44	MECHANICAL



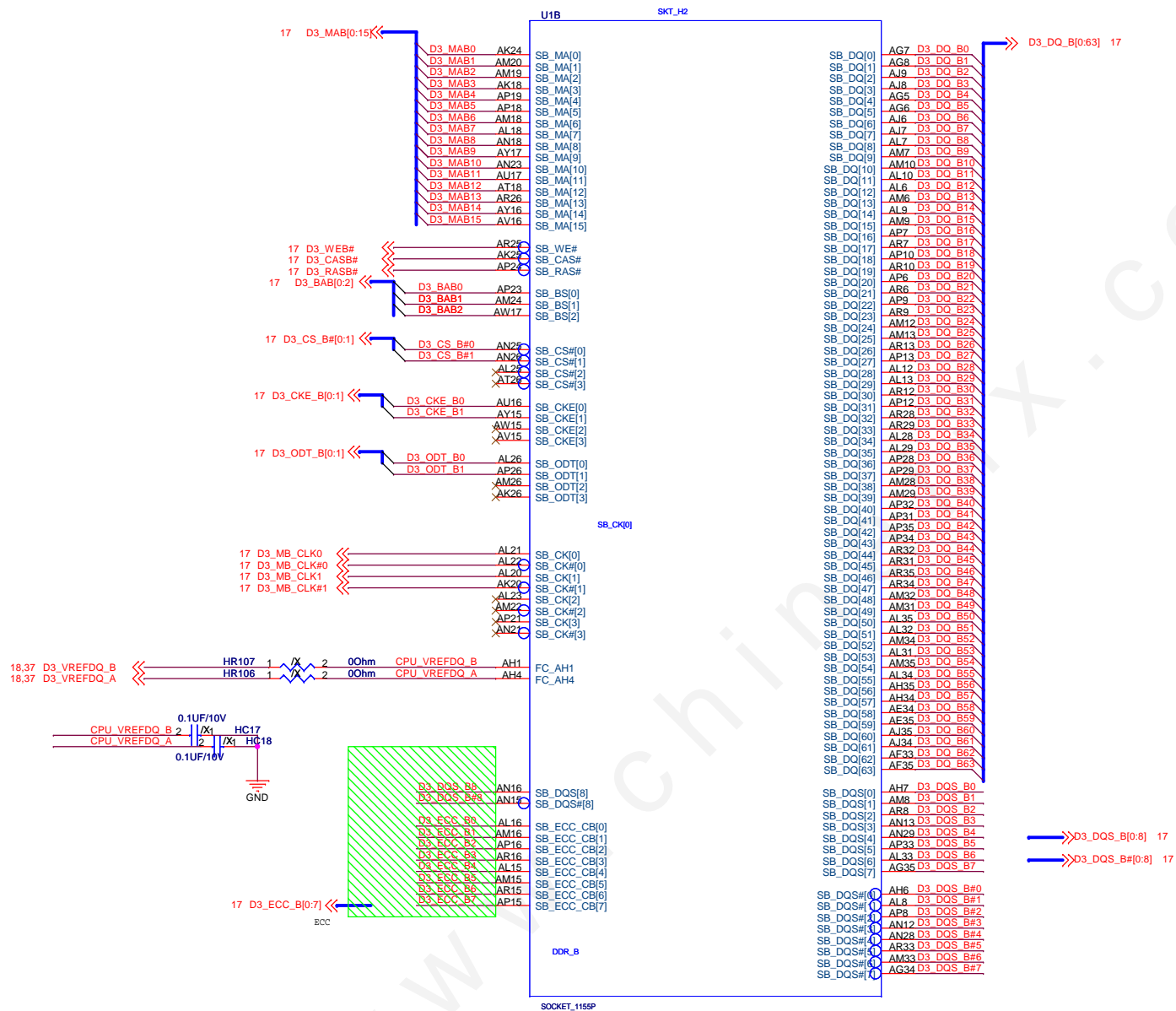
H61MU3S3

NO DATA MASK (DM) on Sandy Bridge Memory Controller!!
Tie DM signals to GND in the DIMM side!!



H61M/U3S3

NO DATA MASK (DM) on Sandy Bridge Memory Controller!!
Tie DM signals to GND in the DIMM side!!

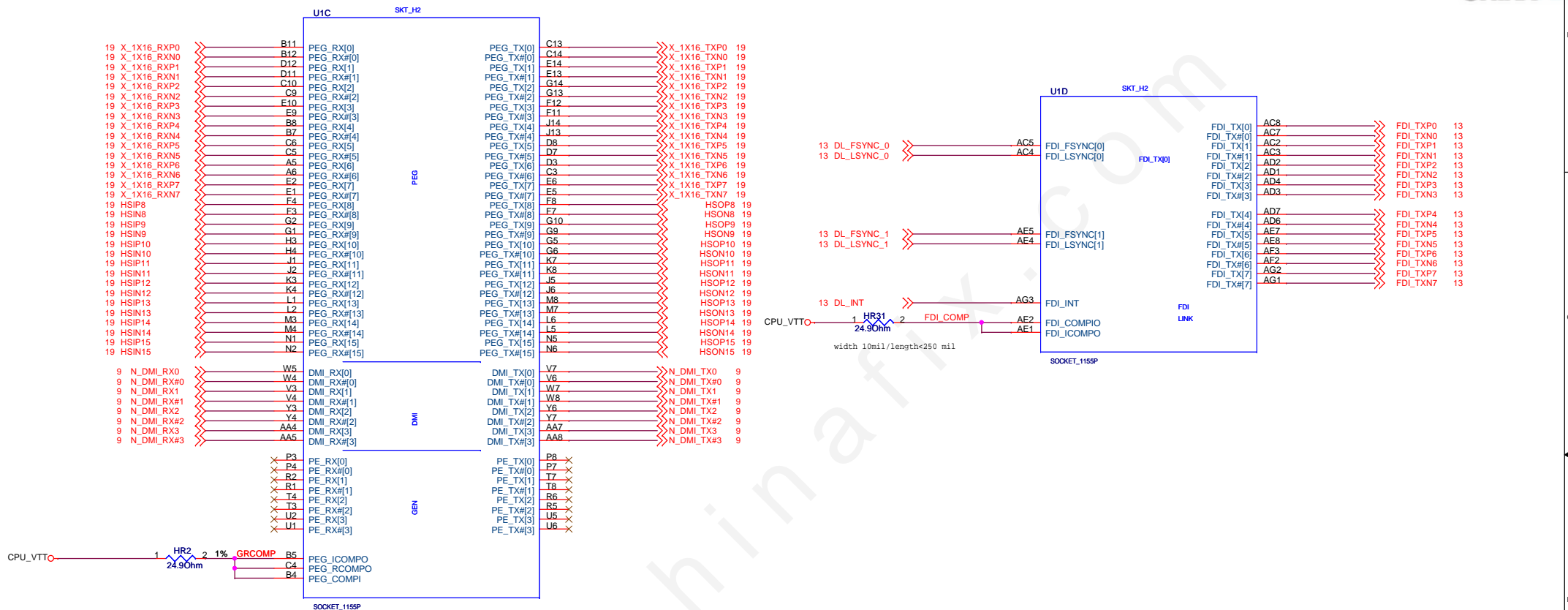


H61M/U3S3

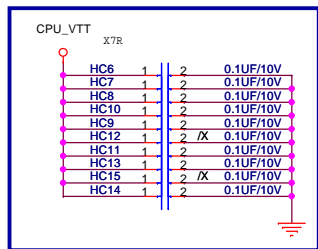
ASRock Inc.		Title : MEM CTRL CHB	
Size		Project Name	
A3		H61M/U3S3	
Date: Tuesday, December 28, 2010		Sheet 3 of 44	
Engineer: Chia-Wei Chang		Rev 1.02	

X_1X16_TXP[0:7] 19
 X_1X16_TXN[0:7] 19
 X_1X16_RXP[0:7] 19
 X_1X16_RXN[0:7] 19

19 HSOP[8:15]
 19 HSON[8:15]
 19 HSIP[8:15]
 19 HSN[8:15]



GRCOMP<500mil
 U1.B4 and U1.C4 tight together then use 4 mil trace to HR2.2
 U1.B5 use 10 mil trace separate to HR2.2



for PCIE signal trans-layer decoupling capacitors!!!
 Place near trans-layer vias for PCIE lanes.

H61M/U3S3

can not connect to clock gen. must be provided by PCH.

2000 mil <U1.AJ19 to HR45 <3000 mil

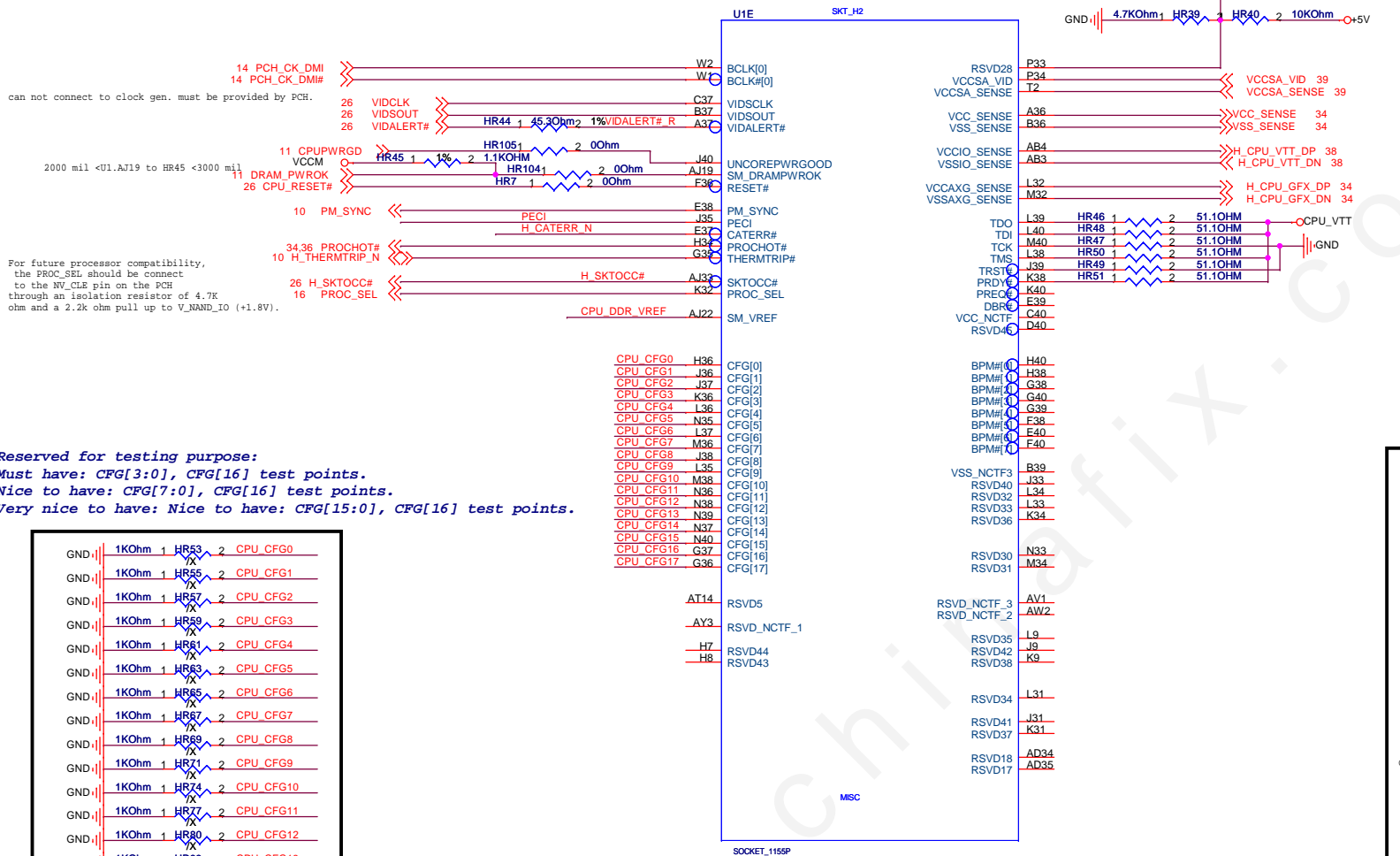
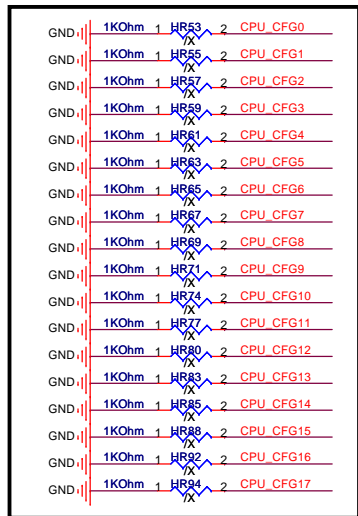
For future processor compatibility,
the PROC_SEL should be connect
to the NV_CLE pin on the PCH
through an isolation resistor of 4.7K
ohm and a 2.2k ohm pull up to V_NAND_IO (+1.8V).

Reserved for testing purpose:

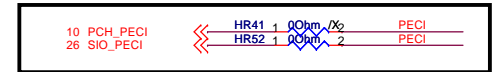
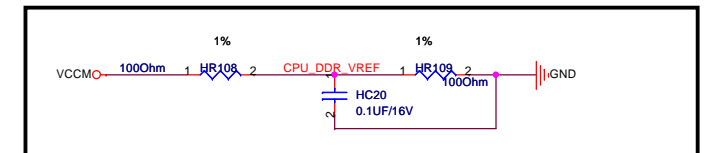
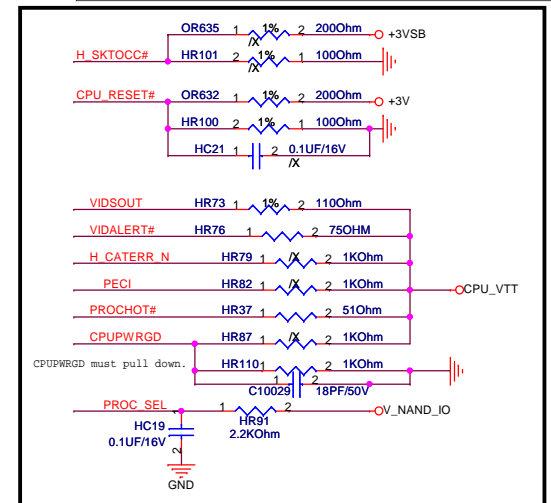
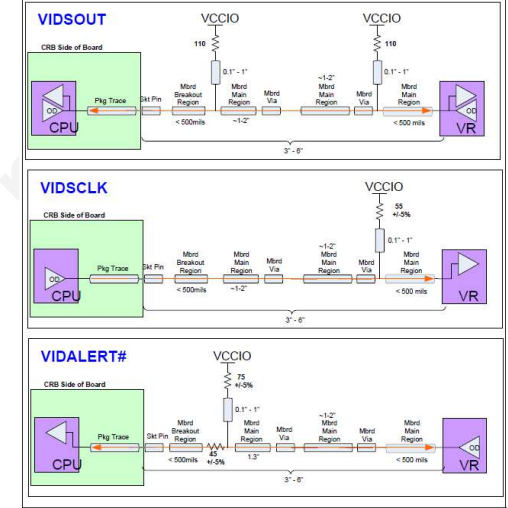
Must have: CFG[3:0], CFG[16] test points.

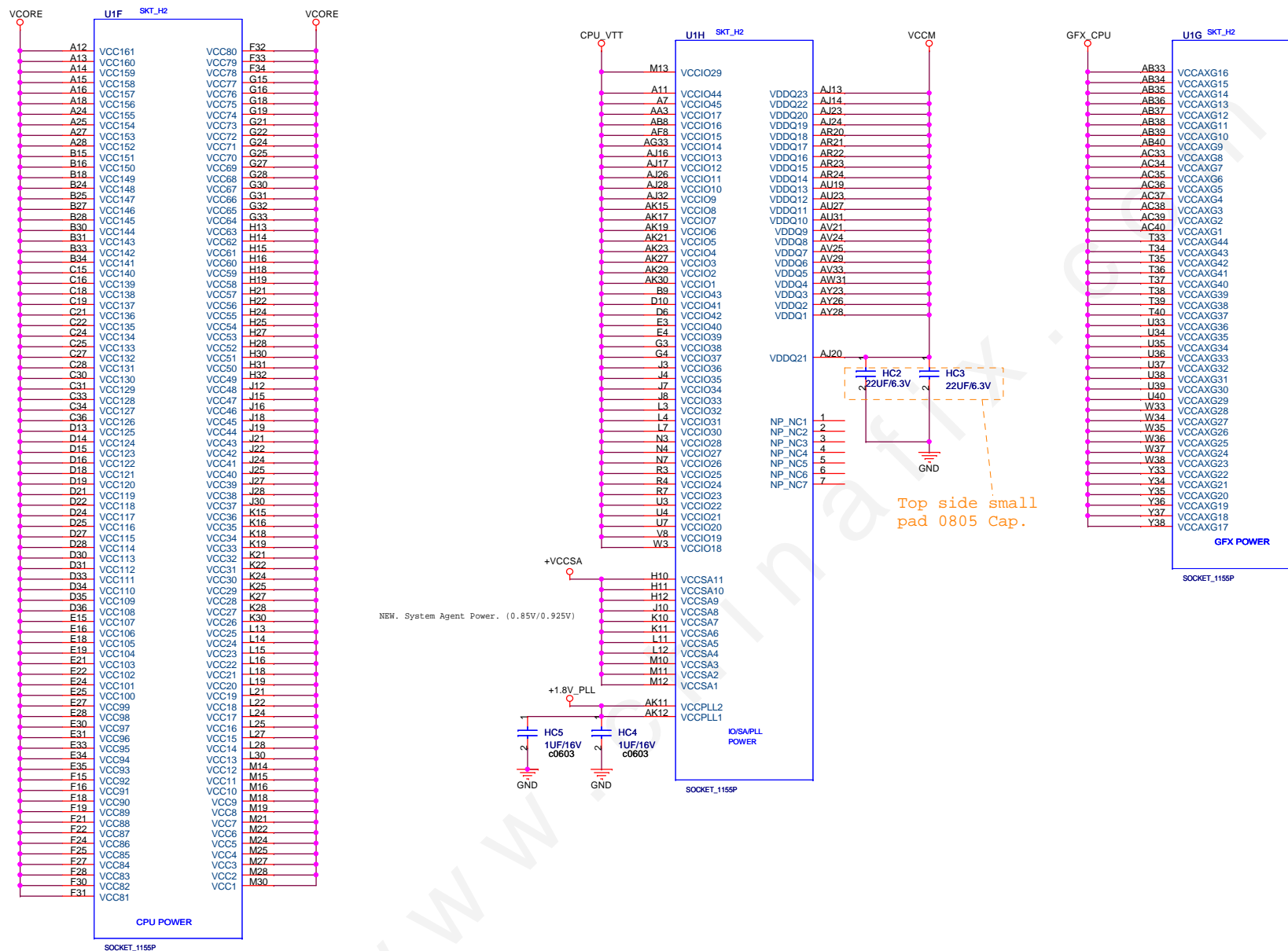
Nice to have: CFG[7:0], CFG[16] test points.

Very nice to have: Nice to have: CFG[15:0], CFG[16] test points.



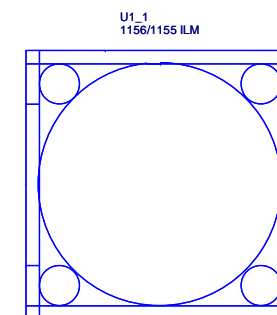
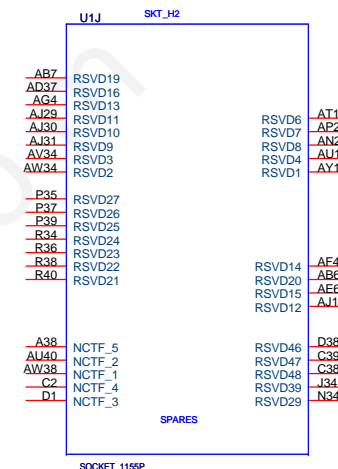
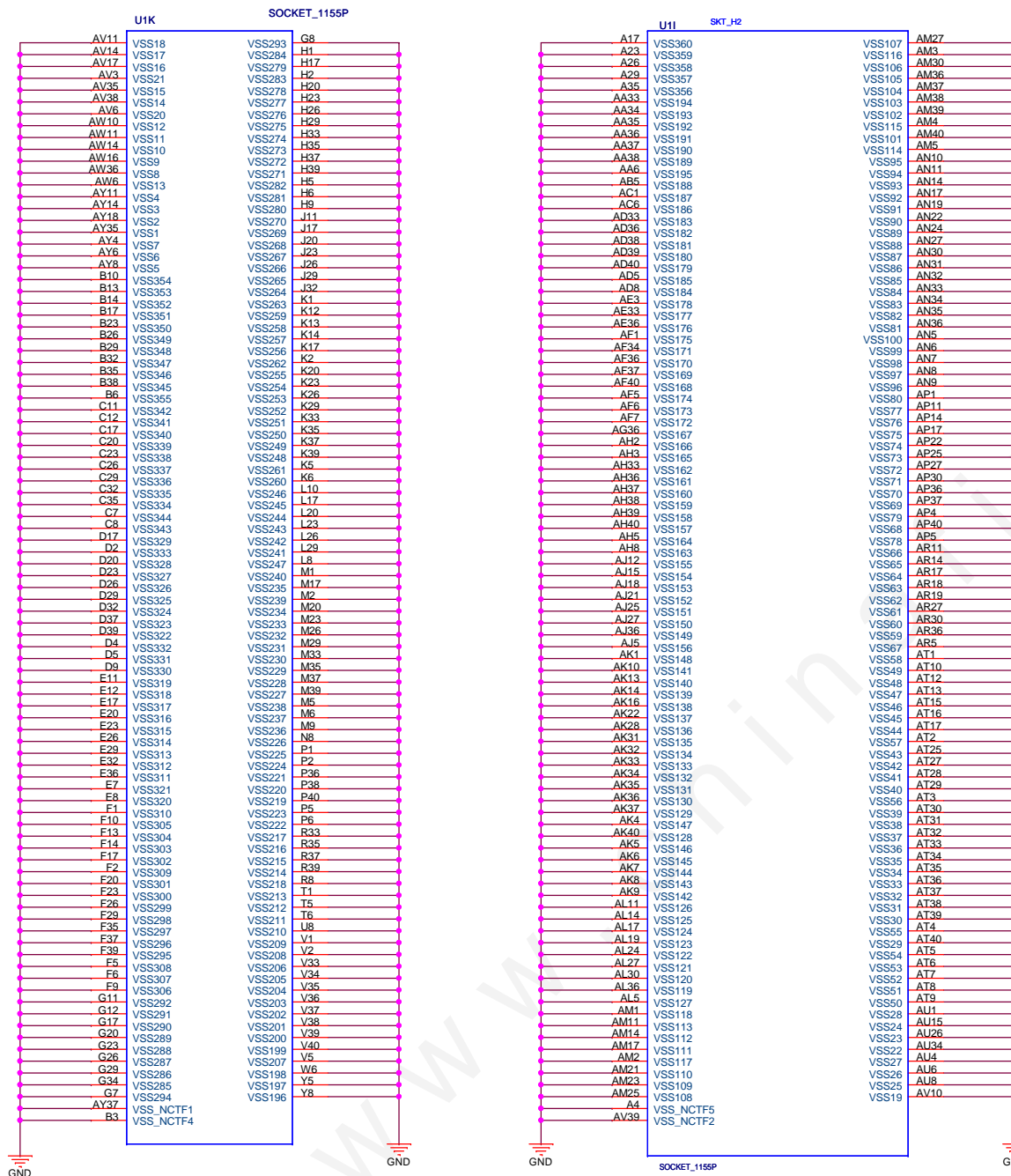
SVID Placement needs to pay attention
for pull up resistors. See PDG page 330.





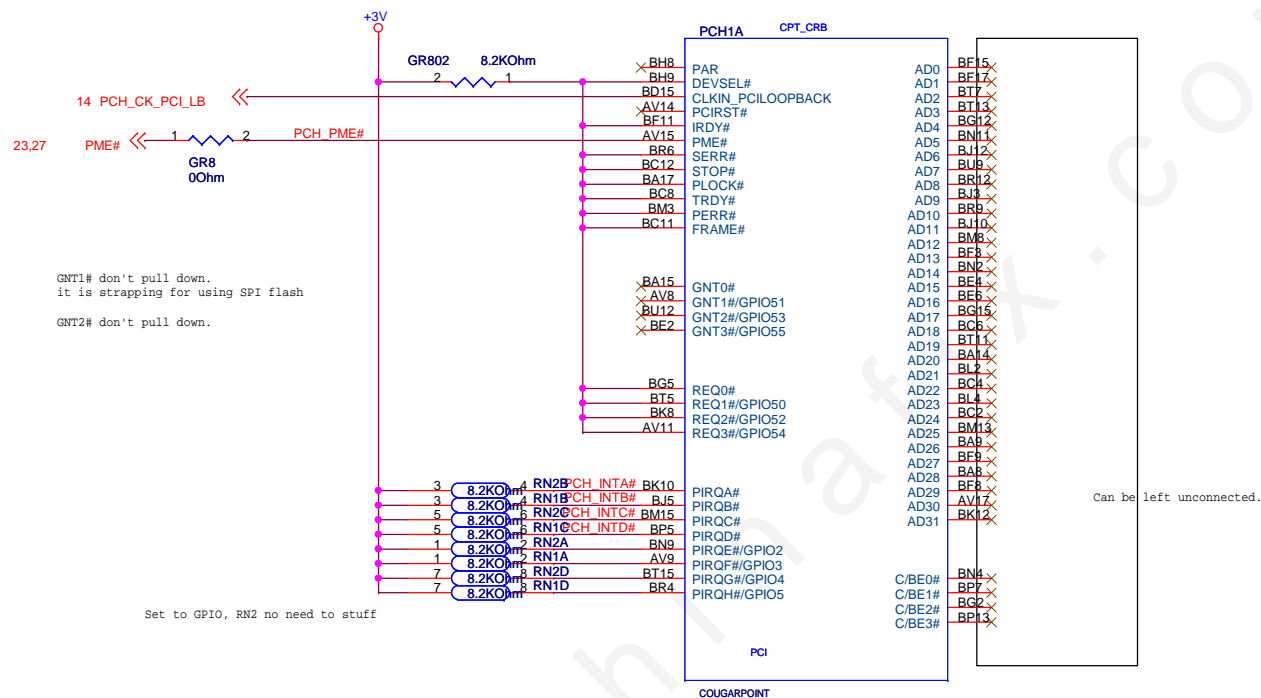
H61M/U3S3

All reserved. No connected.



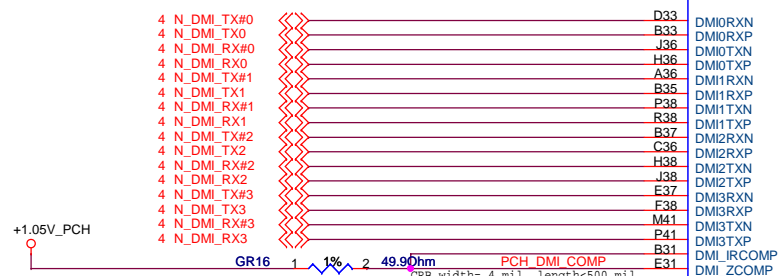
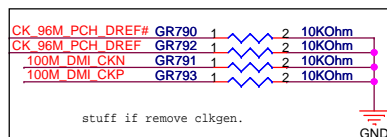
H61M/U3S3

H67/P67/H61 do not support PCI. Check PCI solution!!!

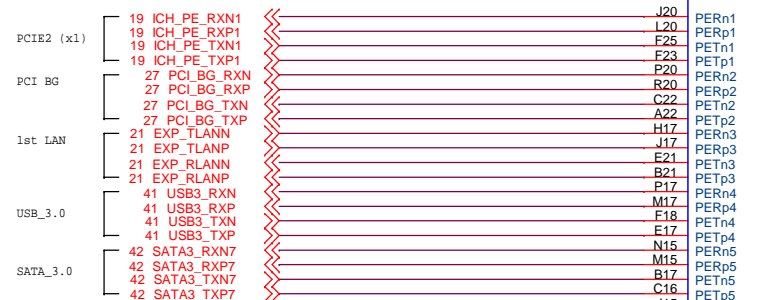


H61MU3S3

ASRock		Title : Clock Distribution	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size B	Project Name H61M/U3S3		Rev 1.02
Date: Tuesday, December 28, 2010		Sheet 8 of 44	

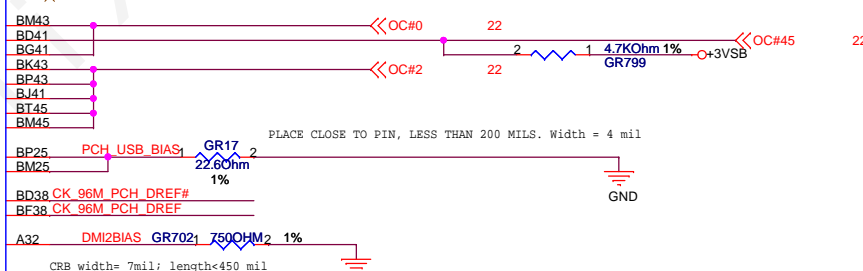
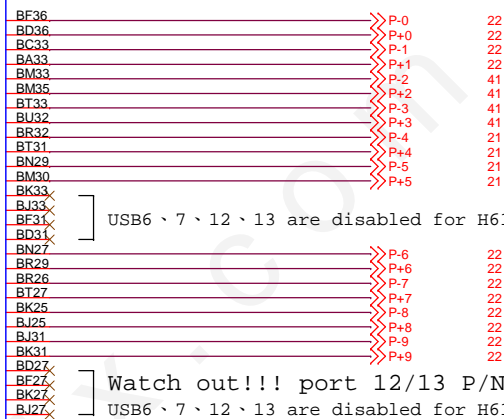
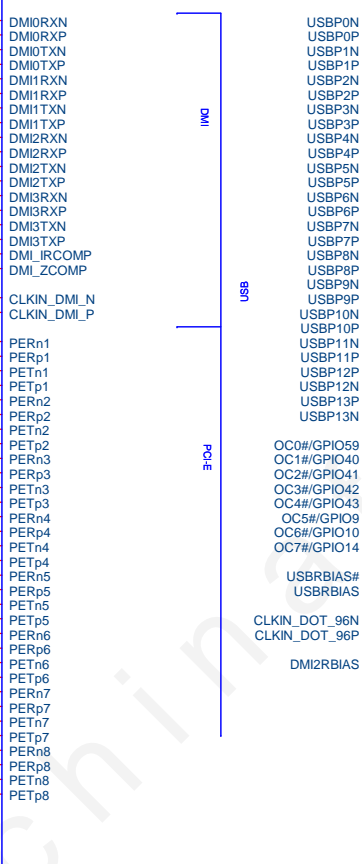


PCIE Port 1 need to connect to Slot.
Do NOT connect to IC.



H61 can not support port 7 & 8

PCH1B CPT_CRB

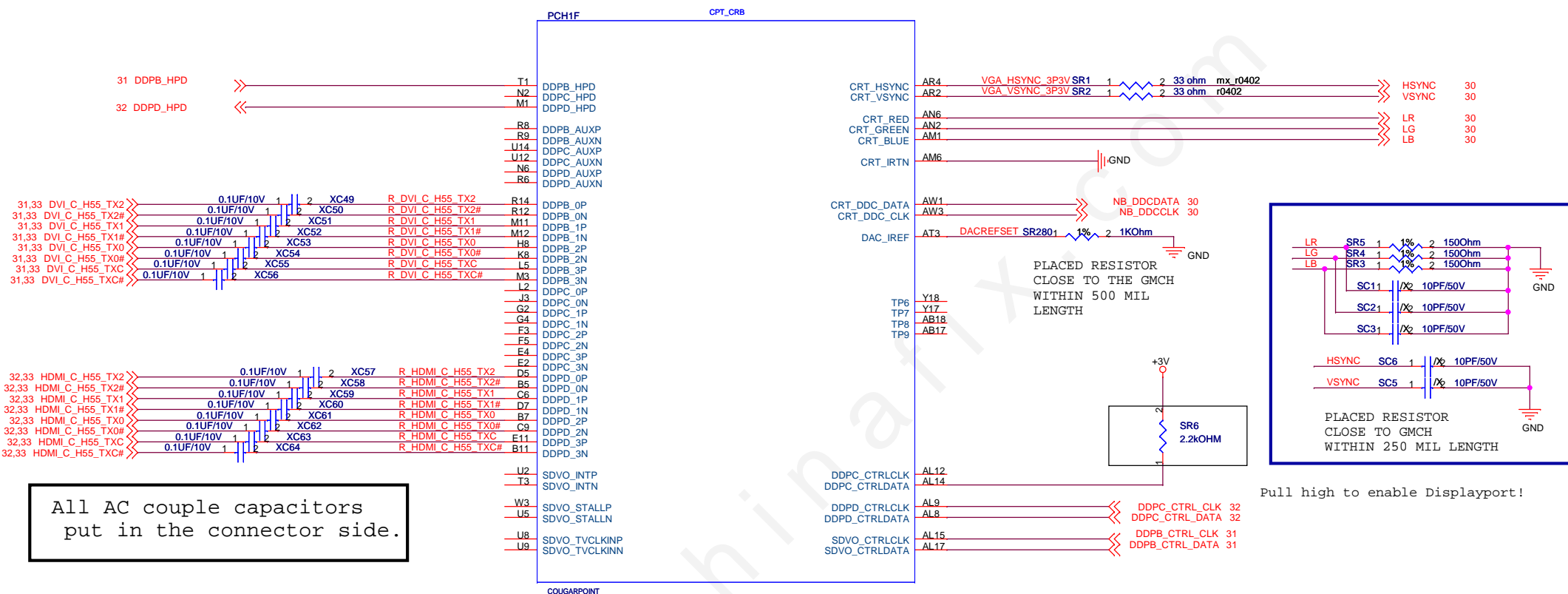


Over Current Pin Default Usage

Pin	Default Port Mapping
OC0#	Port 0, Port 1
OC1#	Port 2, Port 3
OC2#	Port 4, Port 5
OC3#	Port 6, Port 7
OC4#	Port 8, Port 9
OC5#	Port 10, Port 11
OC6#	Port 12, Port 13
OC7#	Not Used

H61MU3S3

ASRock		Title :Clock Distribution	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size B	Project Name H61M/U3S3		Rev 1.02
Date: Tuesday, December 28, 2010		Sheet 9 of 44	



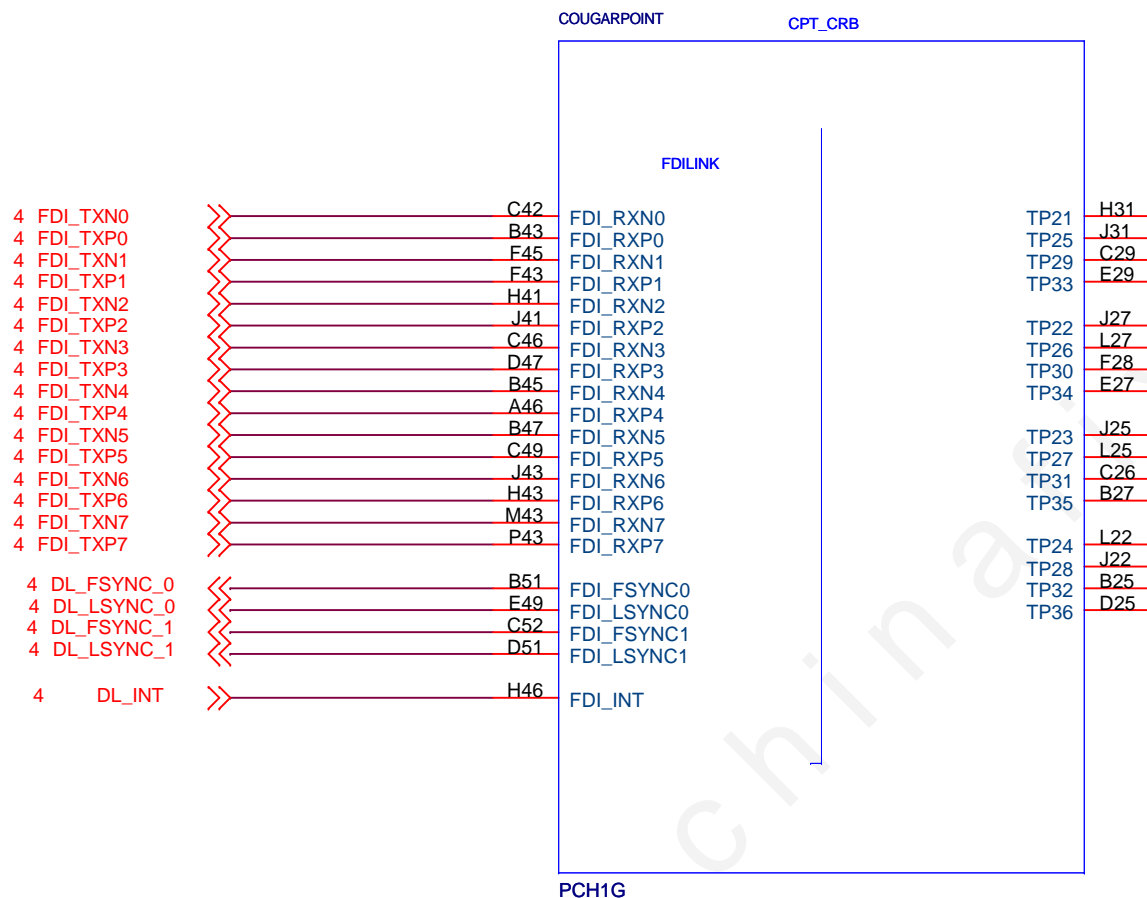
All AC couple capacitors put in the connector side.

- In an effort to address customer display issues more efficiently Intel recommends customers adopt digital display configuration similar to Intel CRB as following


Digital Port	Display Technology
Port B	DVI or SDVO (Desktop) DisplayPort, HDMI/DVI or SDVO (Mobile)
Port C	DisplayPort (Desktop) DisplayPort/HDMI/DVI (Mobile)
Port D	HDMI/DVI/eDP* (Desktop) HDMI/DVI/DisplayPort (Mobile)

H61MU3S3

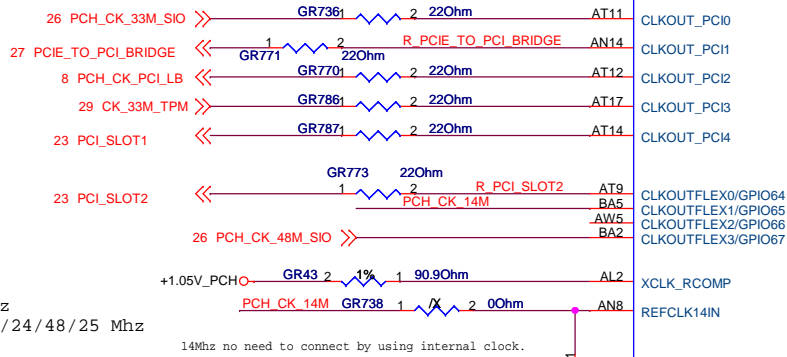
ASRock Title : Clock Distribution	
ASRock Inc. Engineer: Chia-Wei Chang	
Size B	Project Name H61M/U3S3
Date: Tuesday, December 28, 2010	Rev 1.02
Sheet 12	of 44



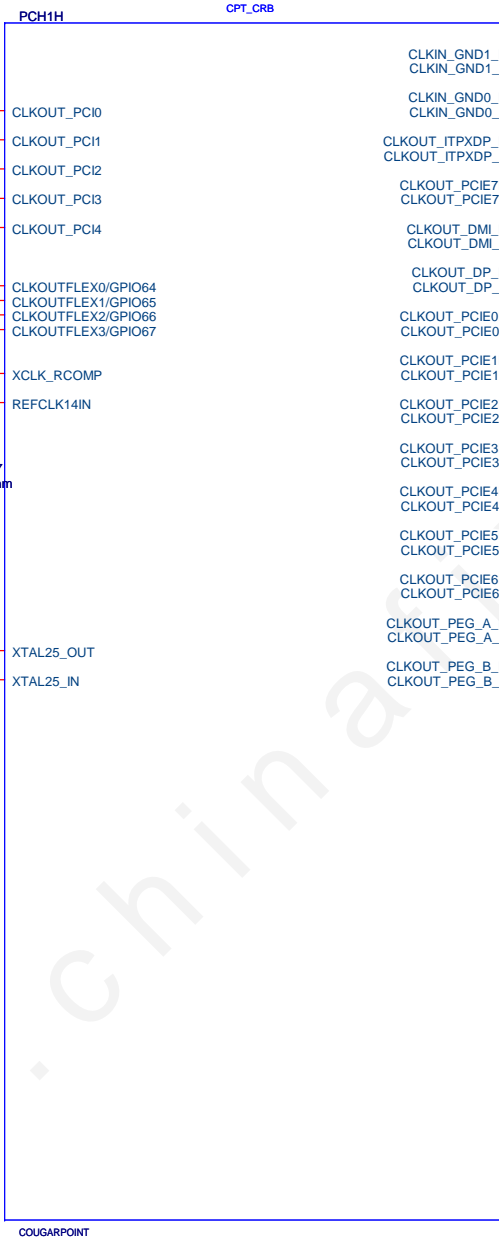
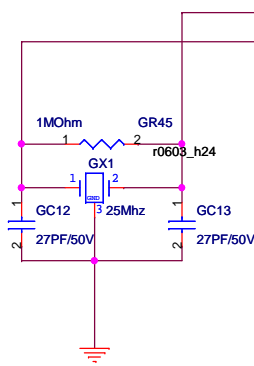
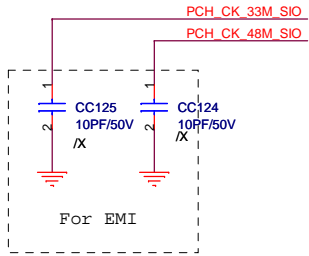
H61M/U3S3

		Title : Clock Distribution	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size A	Project Name H61M/U3S3		Rev 1.02
Date: Tuesday, December 28, 2010		Sheet 13 of 44	


FLEX CLK HAS RULE OF USING.
SEE PDG PAGE 191 FOR DETAILS.

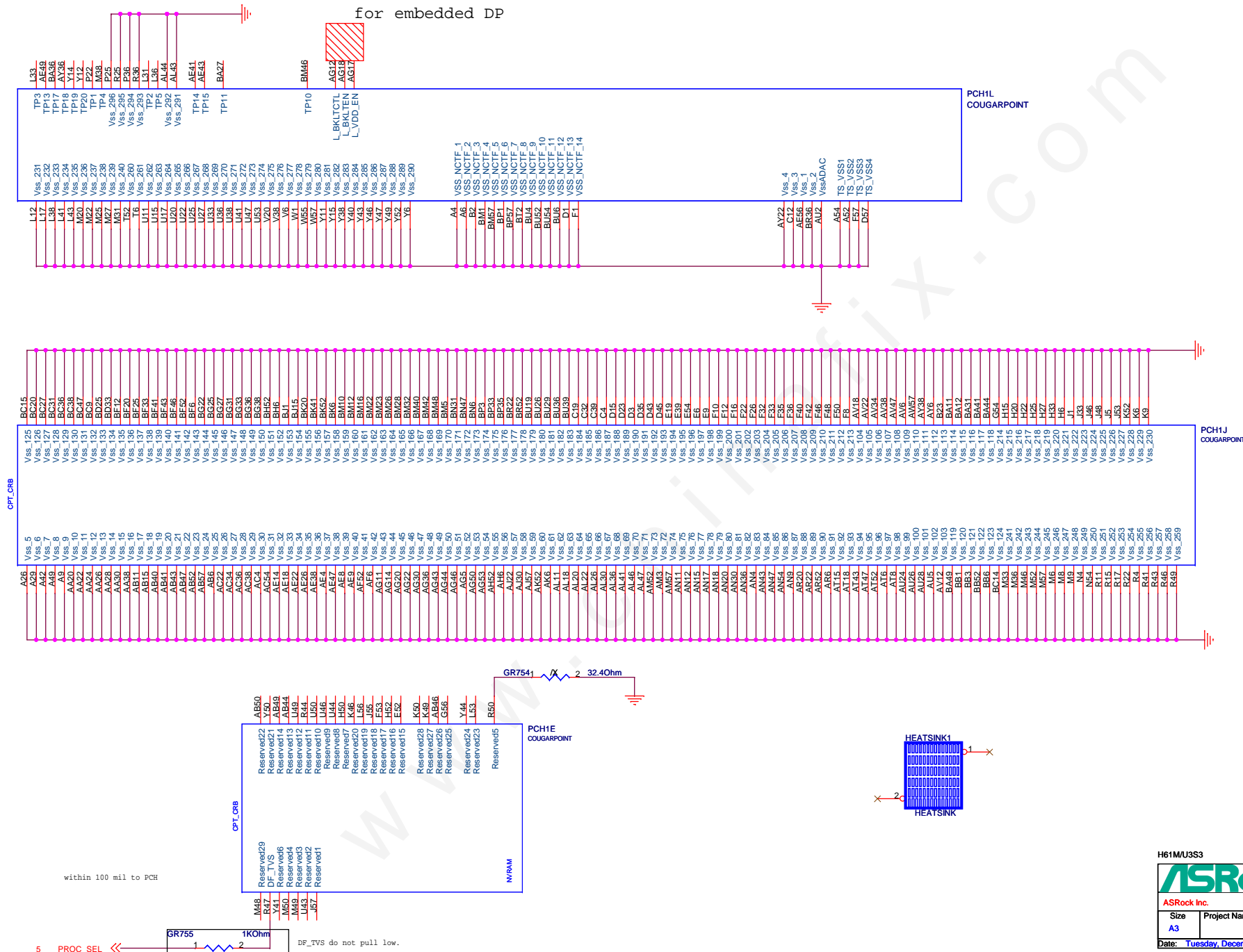


Flex 0, 2 : 33 Mhz
Flex 1, 3 : 27/14/24/48/25 Mhz



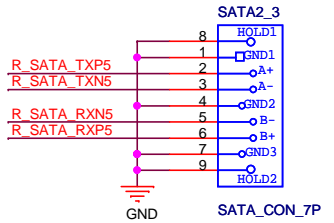
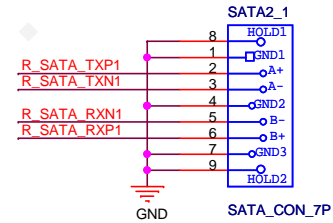
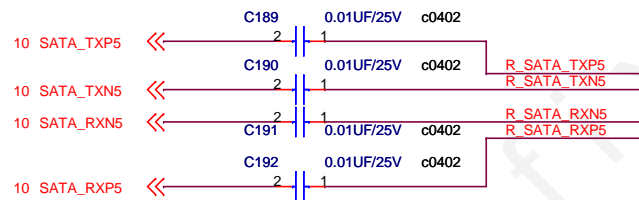
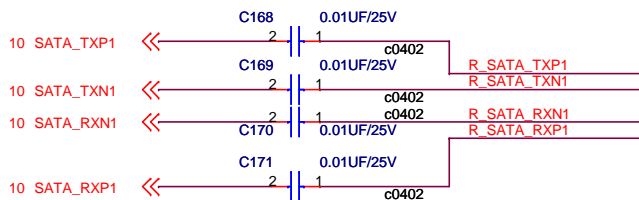
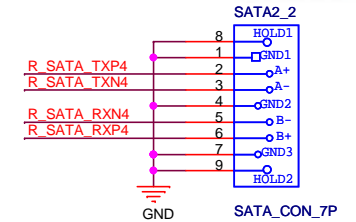
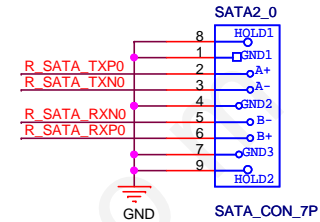
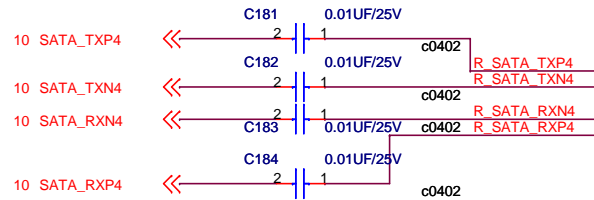
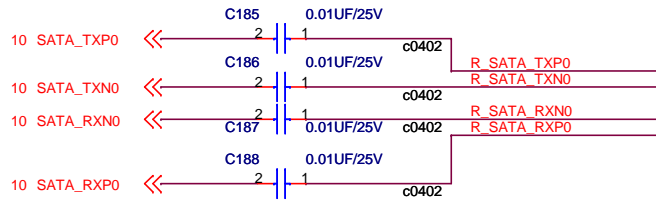
H61M/U3S3

		Title : Clock Distribution	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size B	Project Name H61M/U3S3		Rev 1.02
Date: Tuesday, December 28, 2010	Sheet 14	of 44	

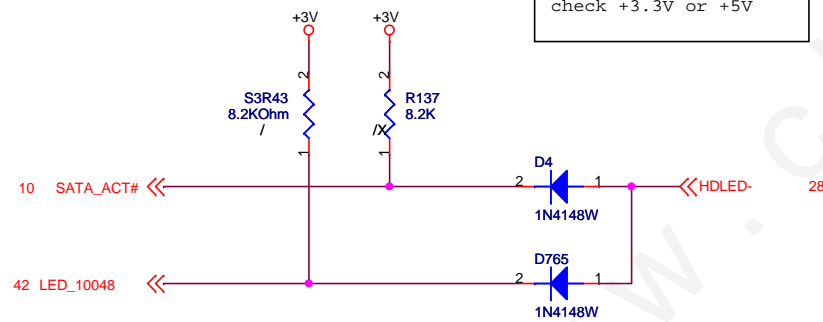


H61M/U3S3

SATA2 PORT



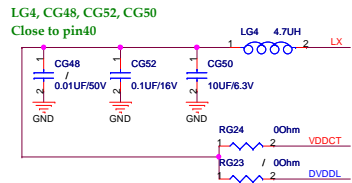
SATA2 LED



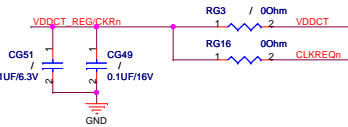
1.00 Internal Pull UP
1.00 If need pul up, check +3.3V or +5V

H61M/U3S3

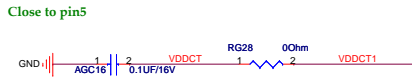
ASRock™		Title : SATA2 port	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size Custom	Project Name H61M/U3S3		Rev 1.02
Date: Tuesday, December 28, 2010		Sheet 20	of 44



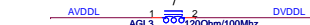
For AR8151 & AR8152: mount RG24, no mount RG23
For AR8161
if AVDDL/DVDDL comes from internal SWR:
mount RG23, LG4, CG52, CG48, CG50, no mount RG24
if AVDDL/DVDDL comes from internal LDO:
no mount RG23, RG24, LG4, CG48, CG52, CG50



For AR8151 & AR8161: mount RG16, no mount RG3, CG51, CG49
For AR8152:
no mount RG16
if center tap power come from internal switch regulator
no mount RG3, CG51, mount LG4, CG48, CG52, CG50, CG49
if center tap power come from internal LDO
no mount LG4, CG48, CG52, mount RG3, CG51, CG49, CG50

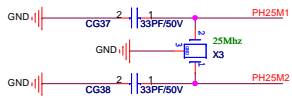


For AR8151 & AR8152: mount RG28, AGC16



For AR8151 & AR8152: no mount AGL3
For AR8161: SWR: mount L3; LDO: no mount AGL3

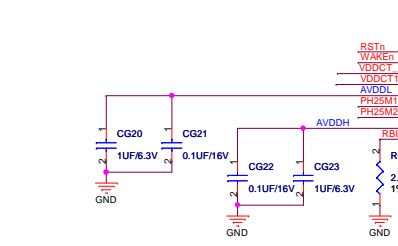
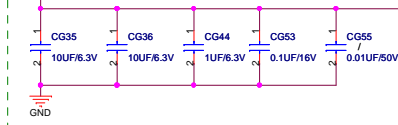
25MHz Crystal



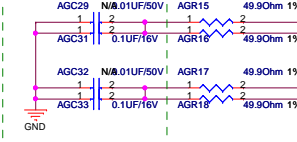
For AR8152 & AR8161,
if clock comes from external clock source,
mount AGC57, no mount CG37, CG38, X3
The value of AGC57 depends on the voltage of clock source,
for detailed information, please refer to the design guide.
For AR8151,
mount CG37, CG38, X3, no mount AGC57

If mount AGX1, 25M_CLK_GEN can be delete.

close to pin1

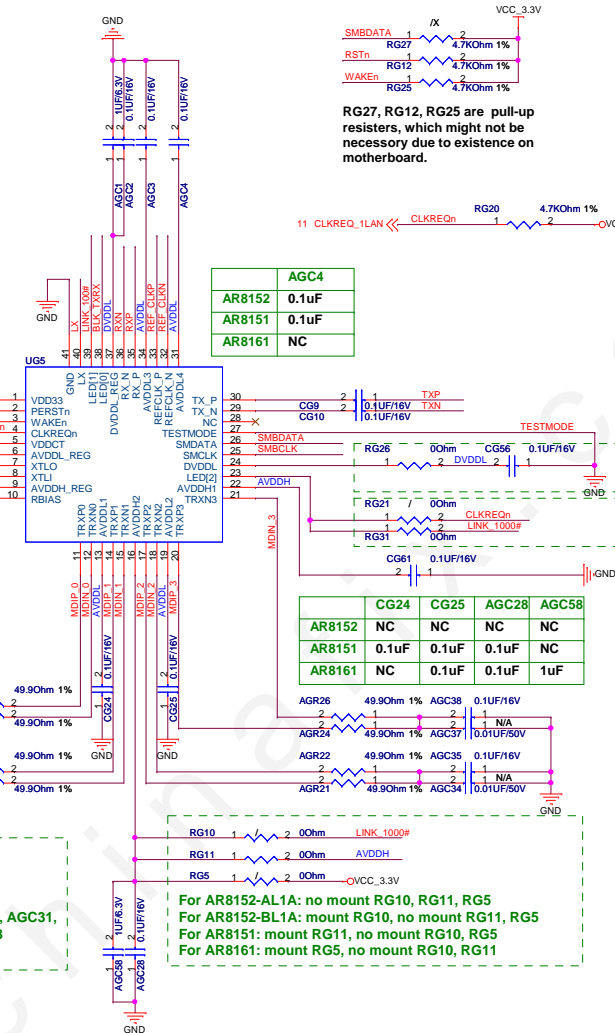
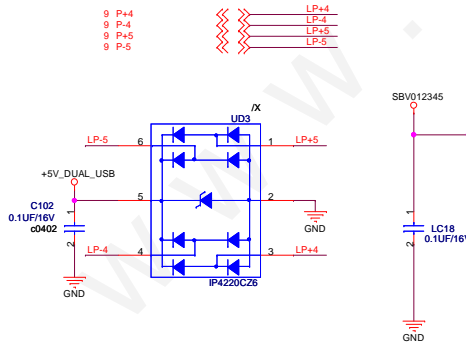


Close to LAN chip
reserved for EMI.



For AR8152, no mount AGR21, AGR22, AGR24,
AGR26, AGC34, AGC35, AGC37, AGC38

For AR8161, no mount AGR15, AGR16, AGR17,
AGR18, AGR21, AGR22, AGR24, AGR26, AGC29, AGC31,
AGC32, AGC33, AGC34, AGC35, AGC37, AGC38



AGC4	
AR8152	0.1uF
AR8151	0.1uF
AR8161	NC

CG24	CG25	AGC28	AGC58
AR8152	NC	NC	NC
AR8151	0.1uF	0.1uF	NC
AR8161	NC	0.1uF	1uF

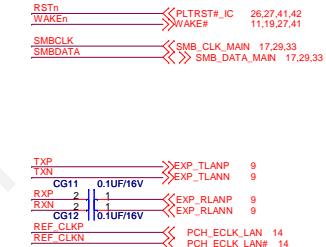
For AR8152-AL1A: no mount RG10, RG11, RG5
For AR8152-BL1A: mount RG10, no mount RG11, RG5
For AR8151: mount RG11, no mount RG10, RG5
For AR8161: mount RG5, no mount RG10, RG11

SMBDATA 1 1X
RSTn RG27 1 4.7Kohm 1%
WAKEn RG12 1 4.7Kohm 1%
RG25 1 4.7Kohm 1%

RG27, RG12, RG25 are pull-up resistors, which might not be necessary due to existence on motherboard.

11 CLKREQ_1LAN CLKREQn RG20 1 4.7Kohm 1% VCC_3.3V

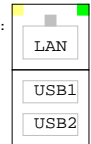
Interface with motherboard



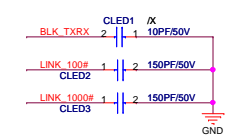
For AR8151 & AR8152: mount RG26, CG56

For AR8152: mount RG21, no mount RG31
For AR8151 & AR8161: mount RG31, no mount RG21

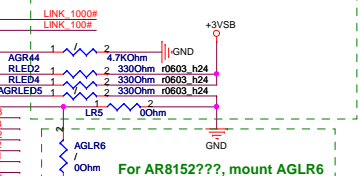
Left LED:
1. YELLOW:
Activity



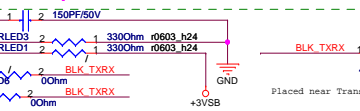
Right LED:
1. GREEN : 1000Mbps
2. ORANGE : 100Mbps
3. No Light : 10Mbps



If using AR8152 in LDO mode, mount AGRLED5

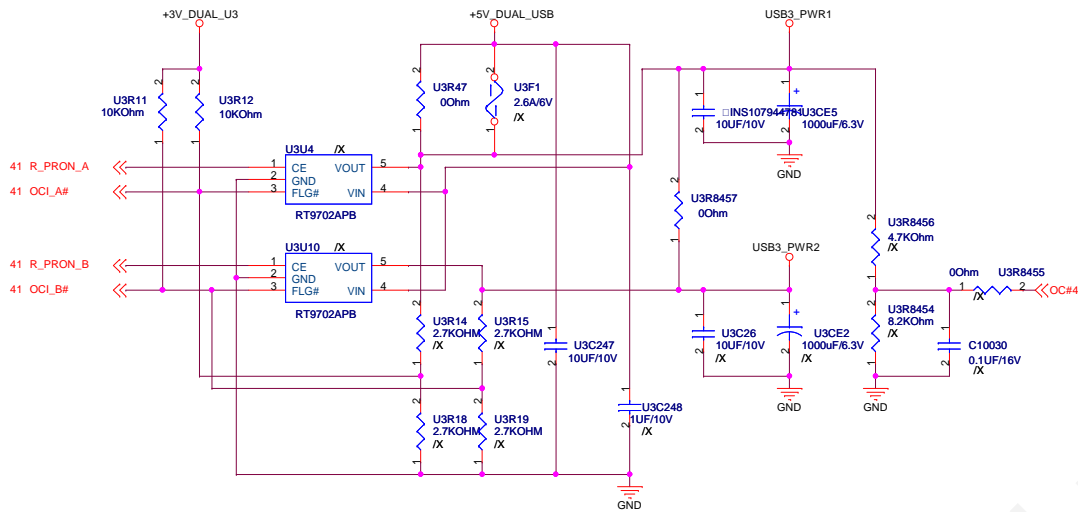
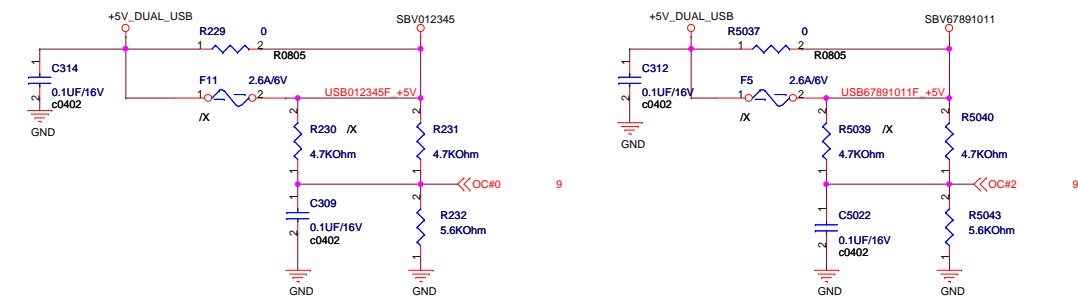


For AR8152???, mount AGLR6

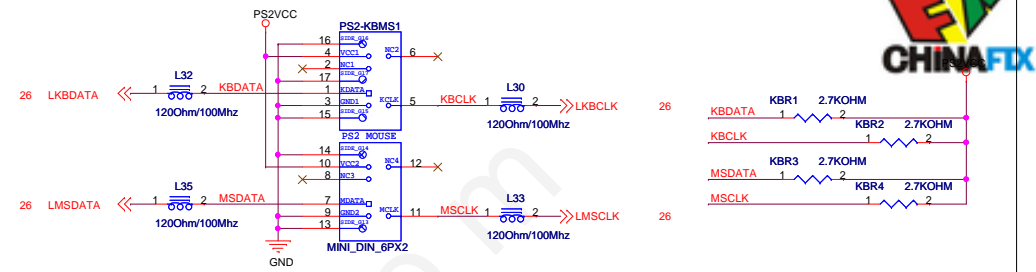


For OC mode: mount RLED1, AGLD6 no mount RLED3, AGLD7, AGR45
For non-OC mode: mount RLED3, AGLD7, AGR45 no mount RLED1, AGLD6

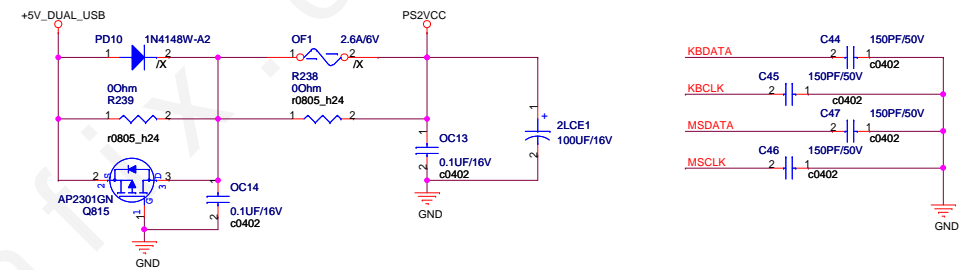
USB Power



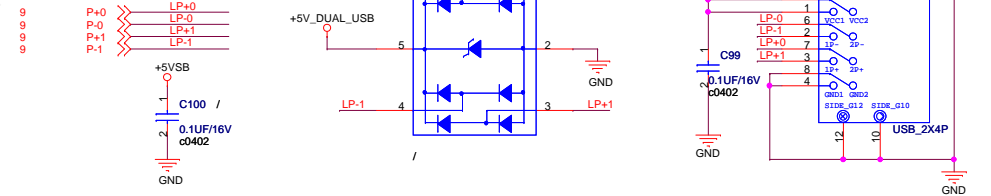
KB & MS



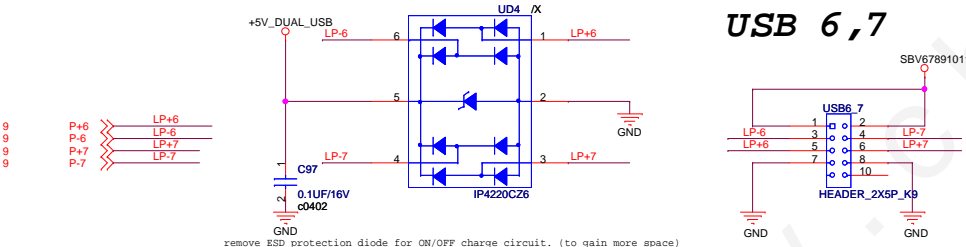
Dual Power



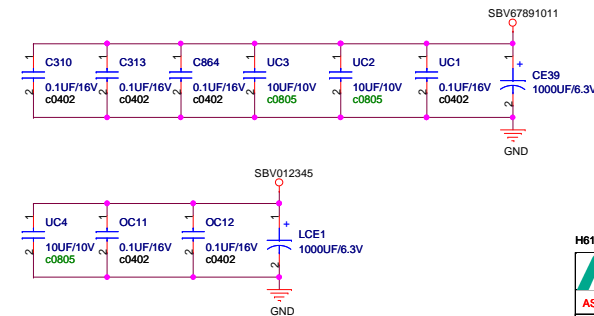
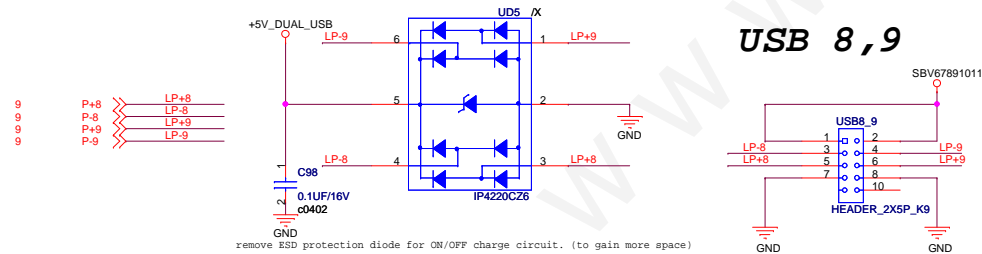
USB 1,2



USB 6,7



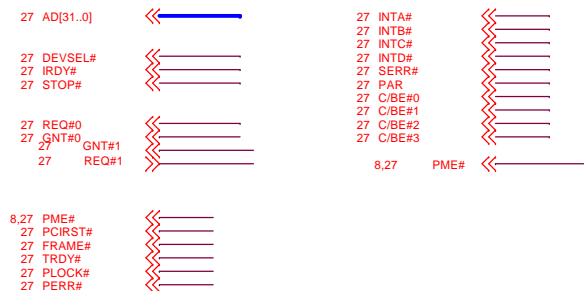
USB 8,9



H61M/U3S3

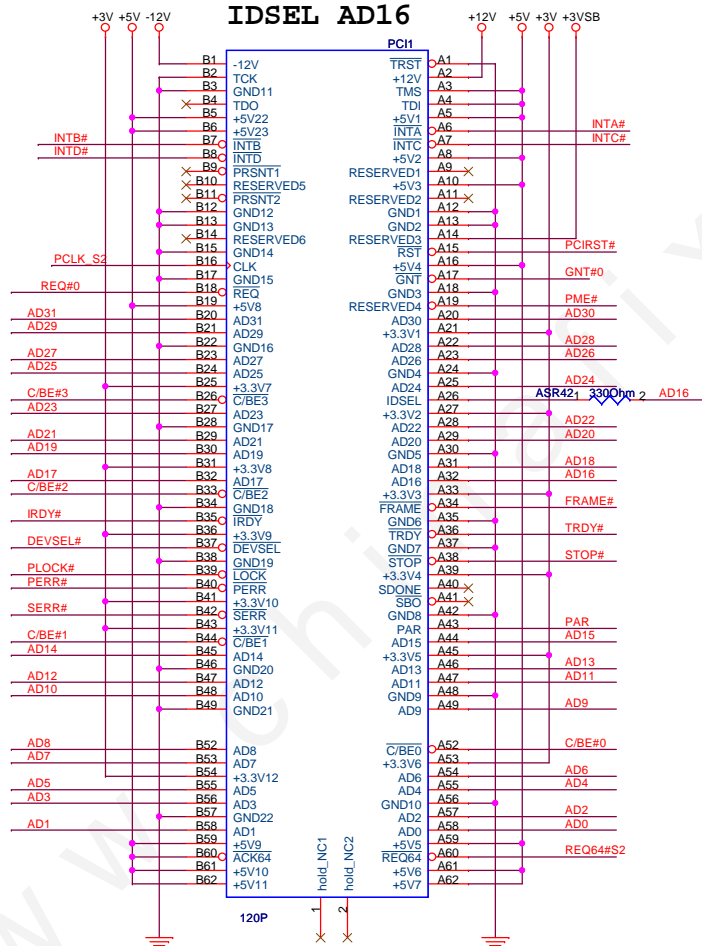
ASRock		Title : USB Port	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size Custom	Project Name H61M/U3S3	Rev 1.02	
Date: Tuesday, December 28, 2010		Sheet 22 of 44	

**THIS IS FOR ASM1083 PCIE TO PCI BRIDGE!!!
DO NOT USE IT FOR SouthBridge!!!**



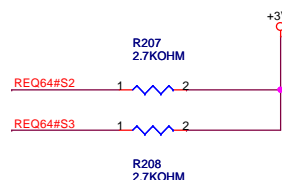
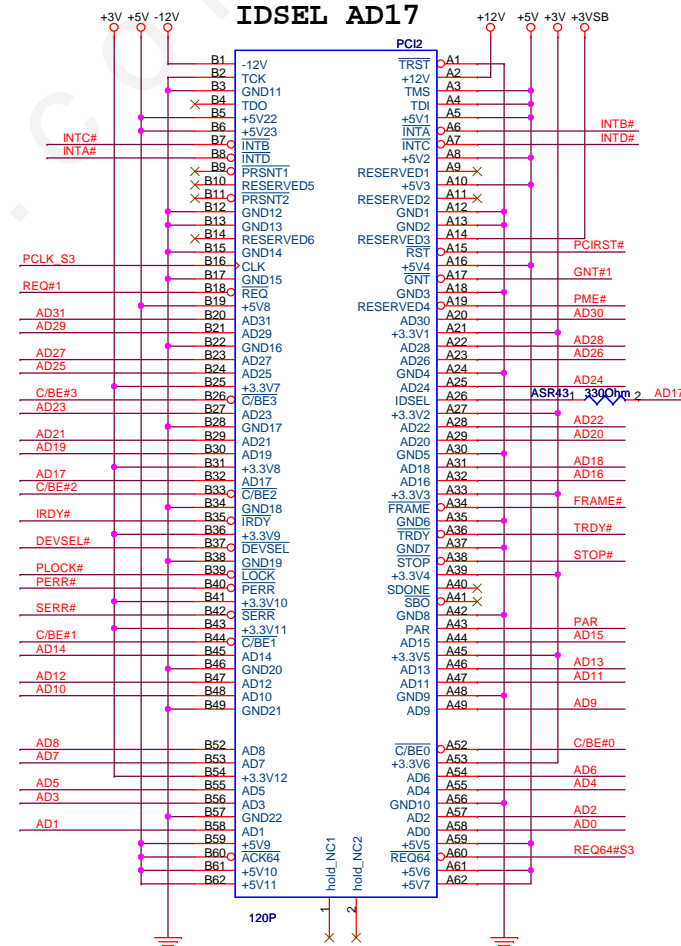
PCI SLOT1

ABCD
IDSEL AD16

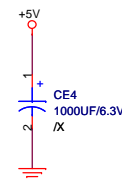


PCI SLOT2

BCDA
IDSEL AD17

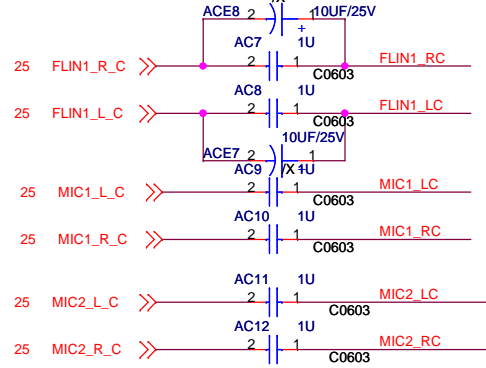
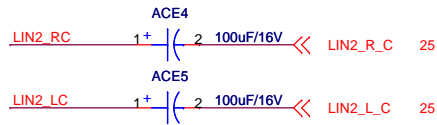


Clock

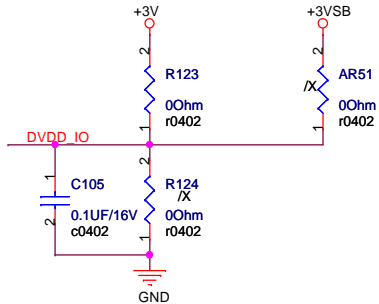
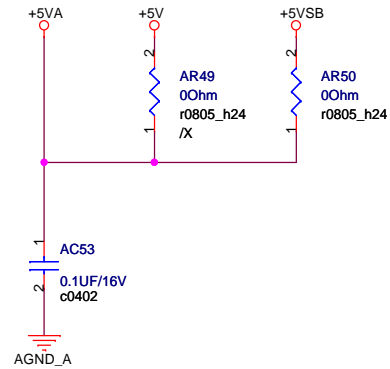


H61M/U3S3

ASRock		Title : PCI Slot	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size A3	Project Name H61M/U3S3	Rev 1.02	
Date: Tuesday, December 28, 2010		Sheet 23 of 44	

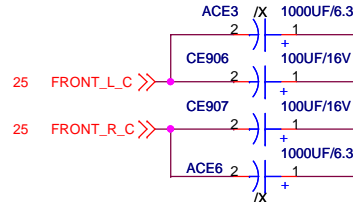


+5V Analog Power Switch

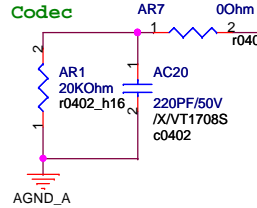


To support Intel HDMI Link, DVDD_IO change to +1.5V(Install R79, uninstall R123)

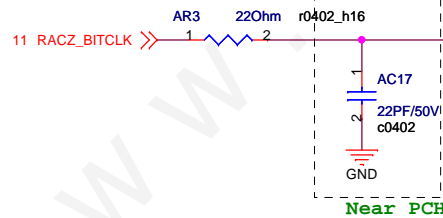
CE906 與 ACE1 Layout需重疊
CE907 與 ACE2 Layout需重疊



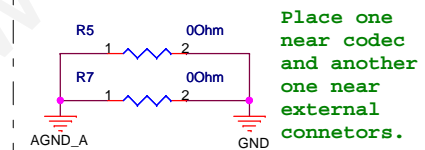
Near Codec



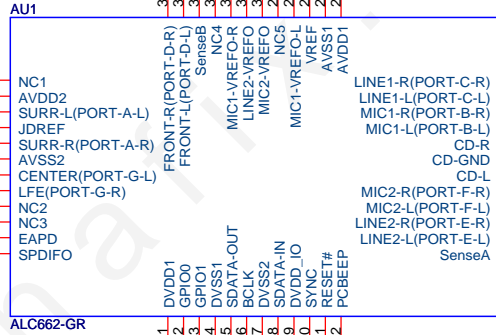
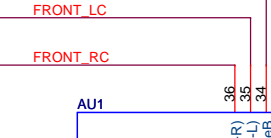
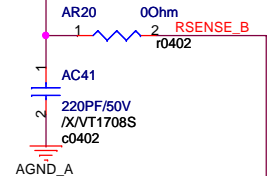
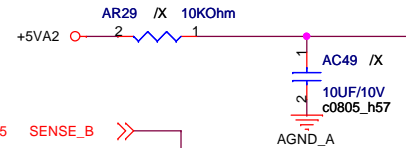
NOTE: ASUS symbol mistake
Pin45: SIDE_L
Pin46: SIDE_R



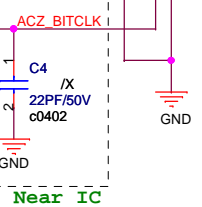
Near PCH



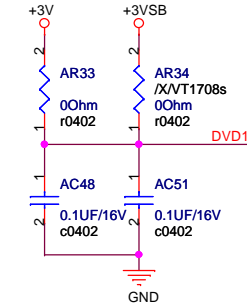
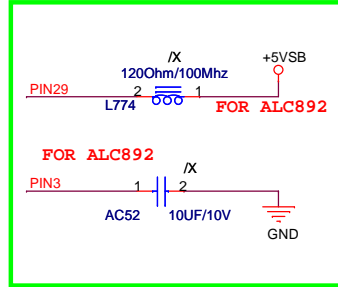
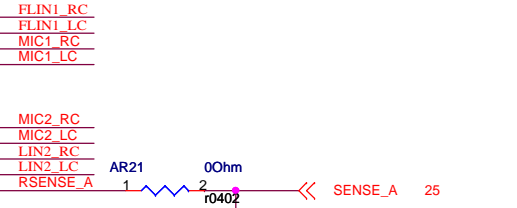
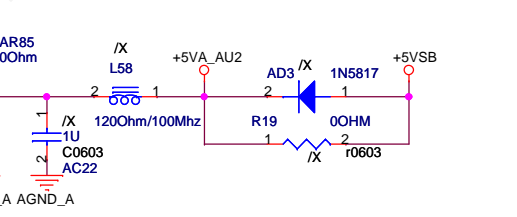
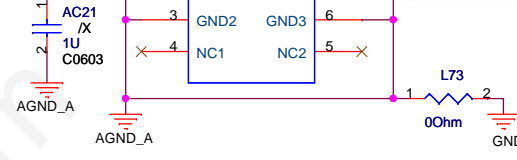
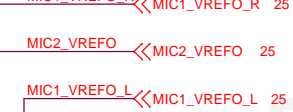
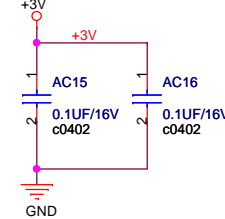
Place one near codec and another one near external connectors.




11 Q_ACZ_SDOUT



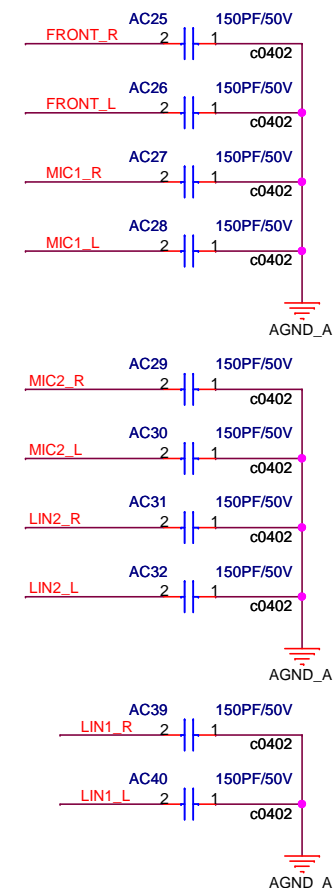
Near IC



H61M/U3S3

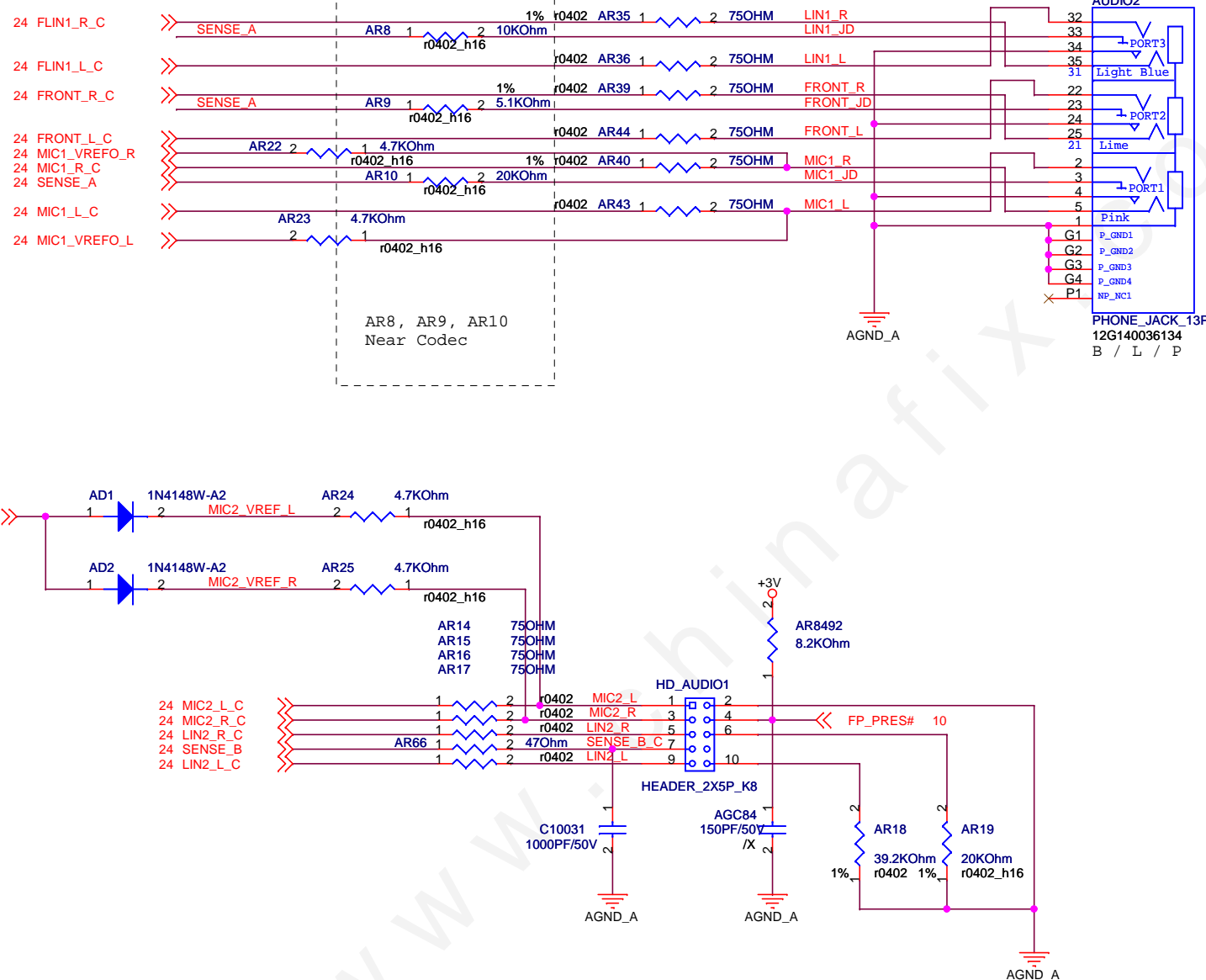
		Title :	ALC662 Codec_1
ASRock Inc.		Engineer:	Chia-Wei Chang
Size Custom	Project Name H61M/U3S3		Rev 1.02
Date: Tuesday, December 28, 2010		Sheet 24	of 44

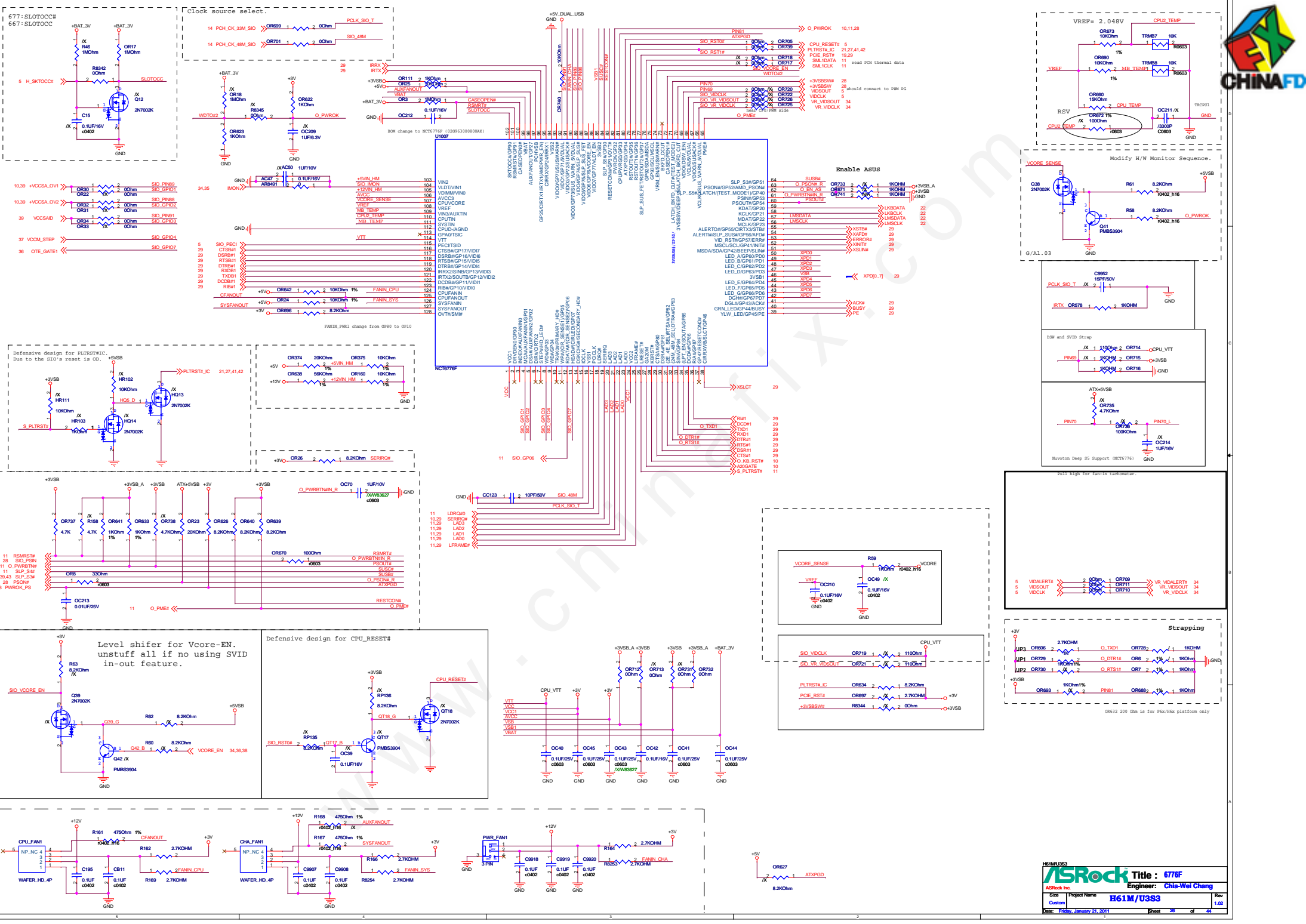
For EMI



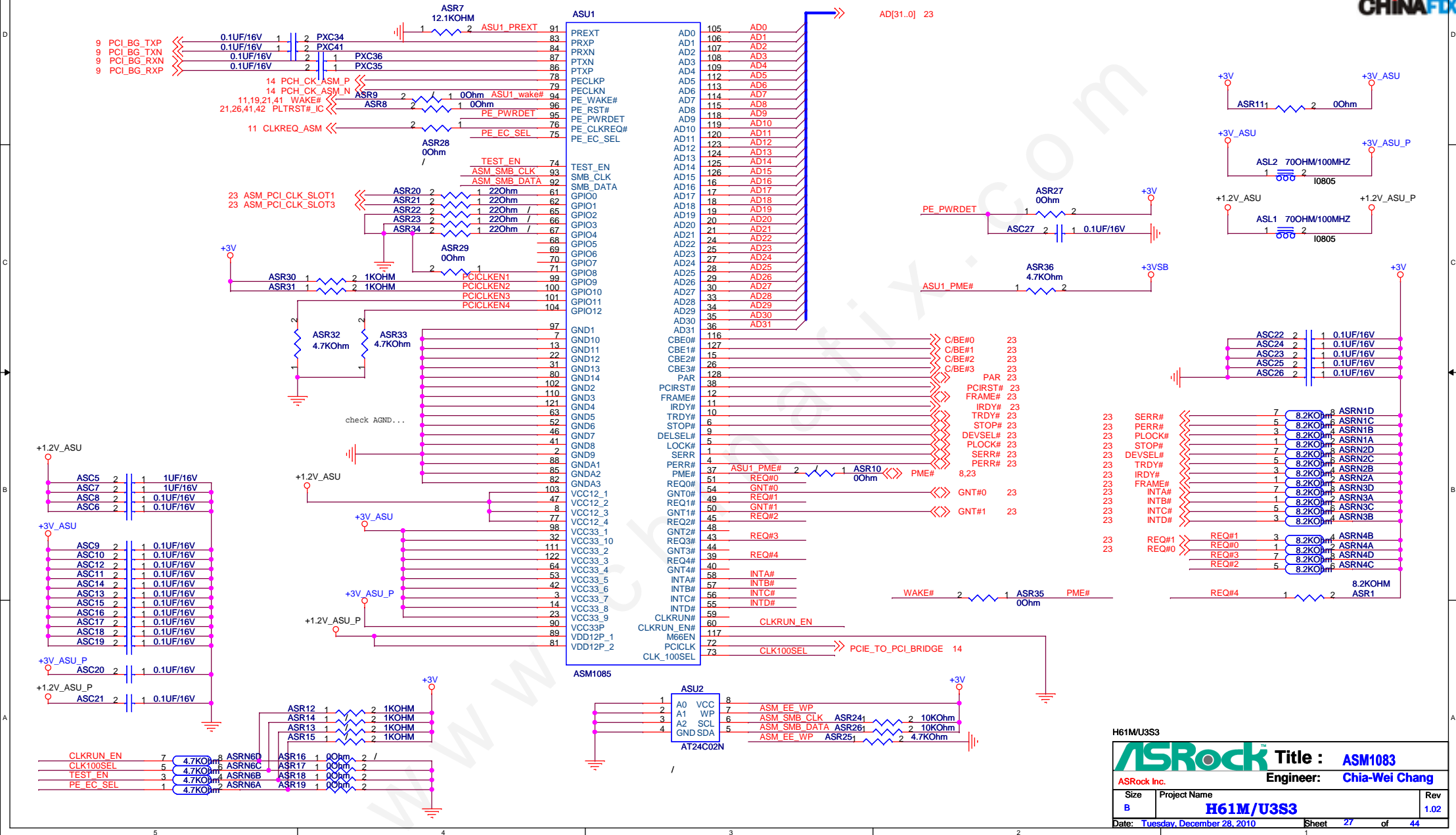
H61MU3S3

ASRock		Title :	ALC662 Codec_2
ASRock Inc.		Engineer:	Chia-Wei Chang
Size Custom	Project Name H61M/U3S3		Rev 1.02
Date: Tuesday, December 28, 2010		Sheet	25 of 44






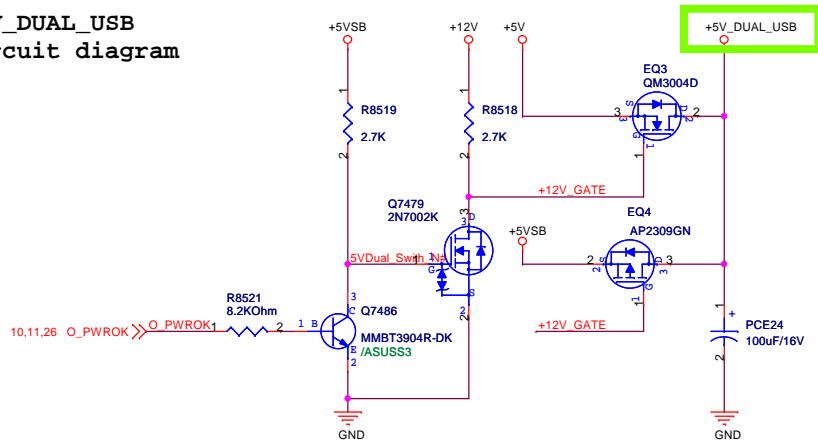
BOM is ASM 1083



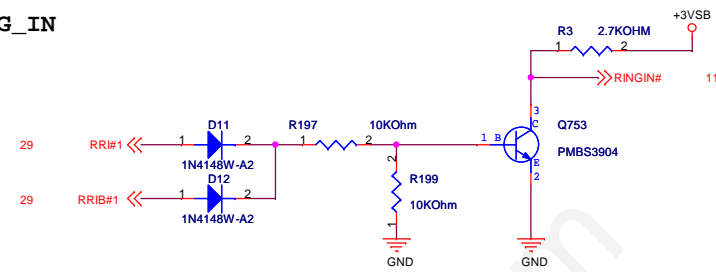
H61M/U3S3

		Title : ASM1083	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size B	Project Name H61M/U3S3		Rev 1.02
Date: Tuesday, December 28, 2010		Sheet 27	of 44

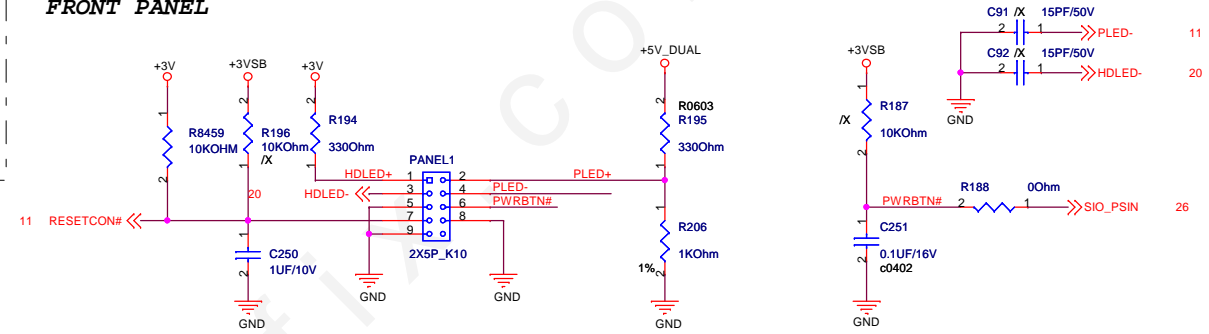
+5V_DUAL_USB circuit diagram



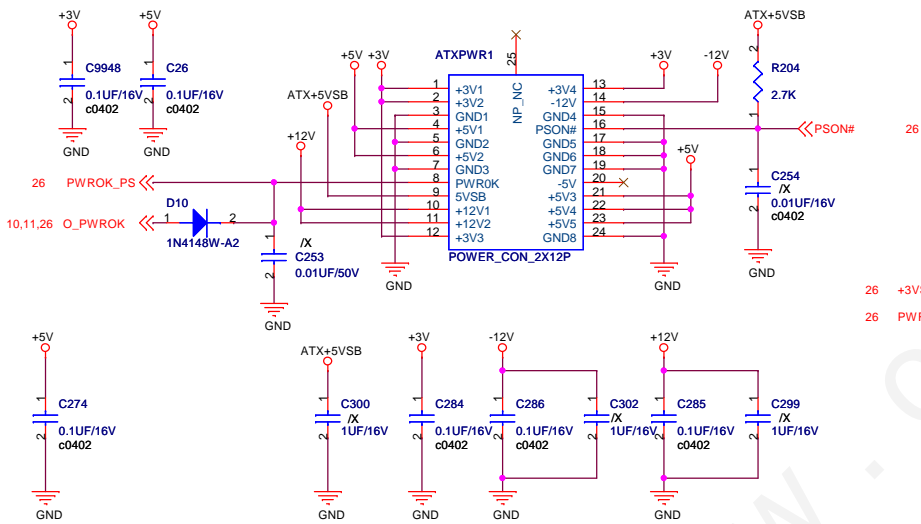
RING_IN



FRONT PANEL

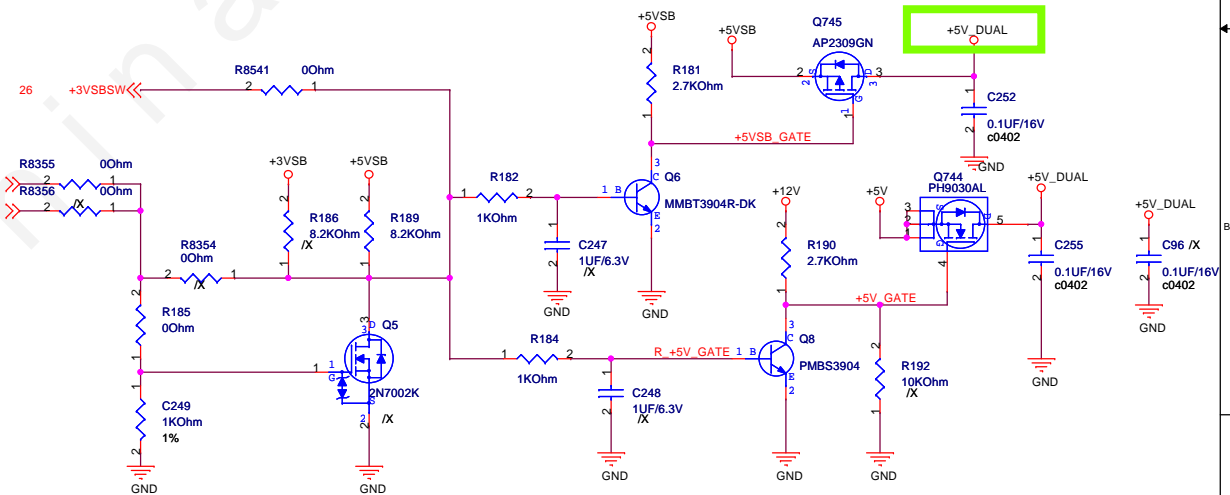


ATXPWR CONN



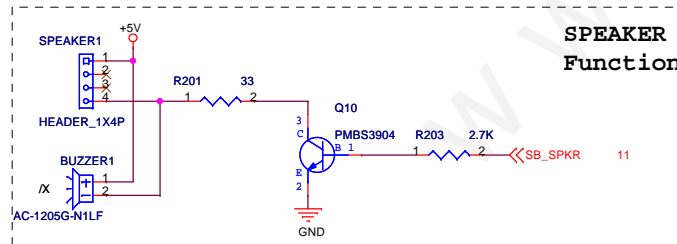
*Around the ATX Power Connector

S3 circuit diagram



Logic IC : R190 = 2.7K, Q8 = 2N7002
BJT : R190 = 8.2K, Q8 = 3904, R192
= uninstall

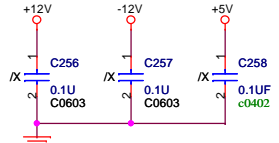
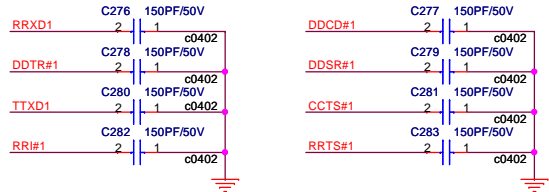
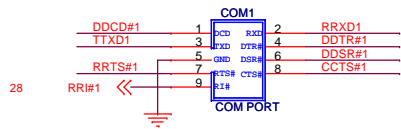
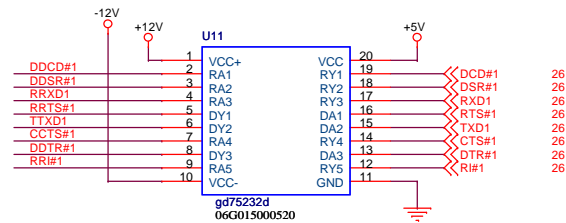
SPEAKER Function



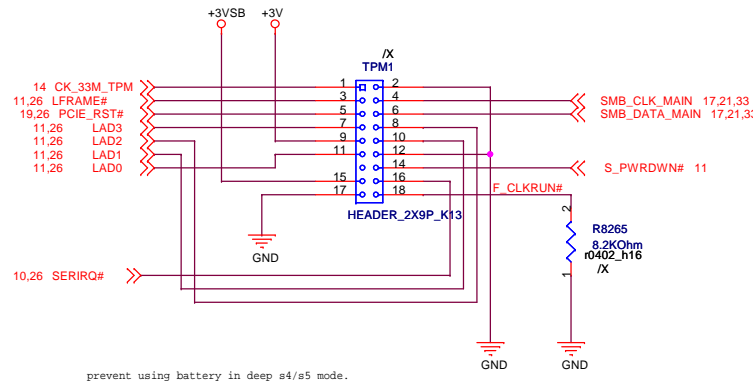
H61M/U3S3

ASRock		Title : POK DUALSW_ENASUS	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size A3	Project Name H61M/U3S3	Rev 1.02	
Date: Tuesday, December 28, 2010		Sheet 28	of 44

COM 1

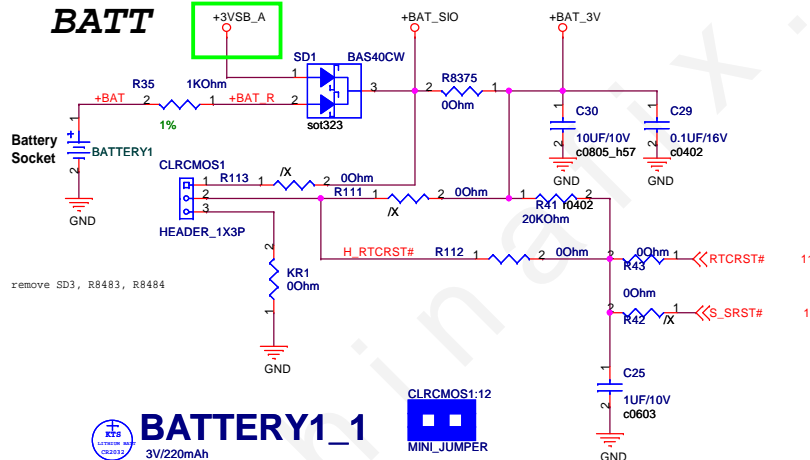


TPM



prevent using battery in deep s4/s5 mode.

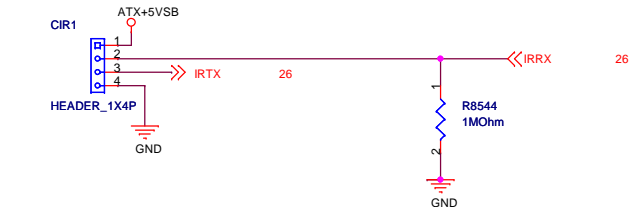
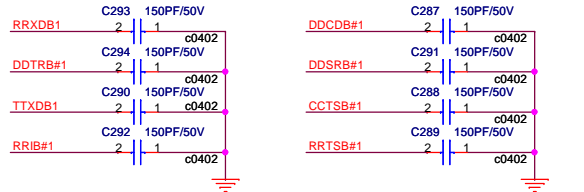
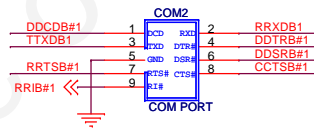
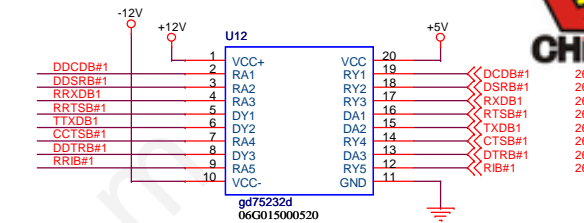
BATT



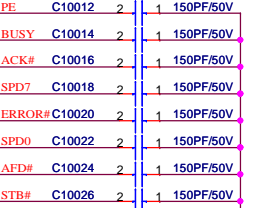
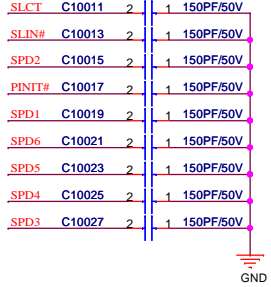
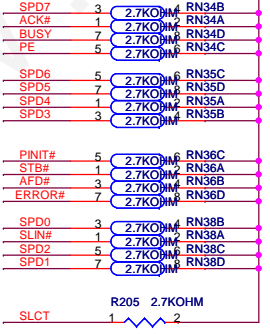
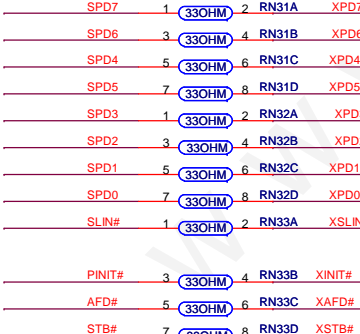
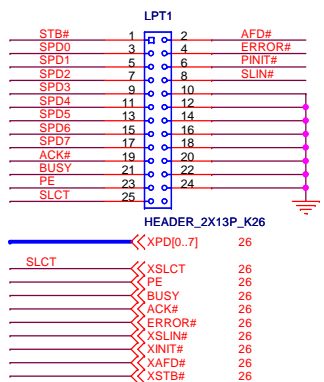
remove SD3, R8483, R8484



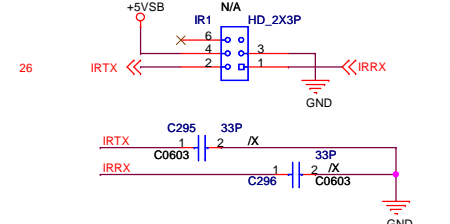
COM 2

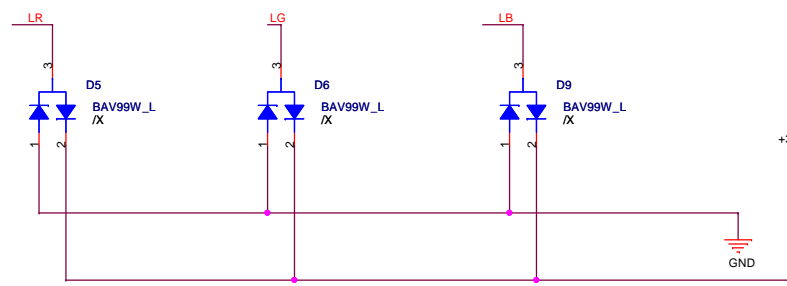
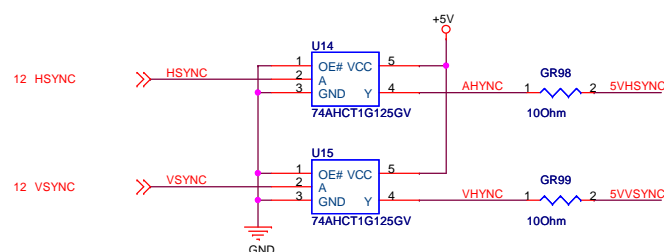
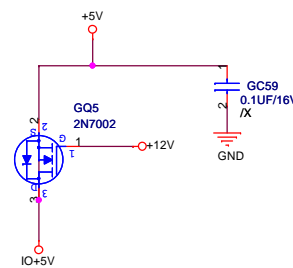
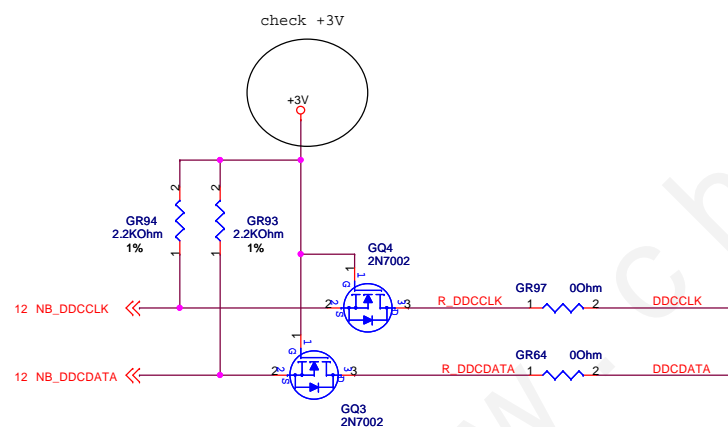
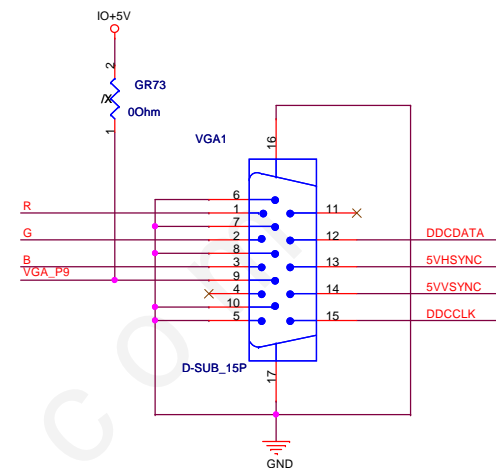
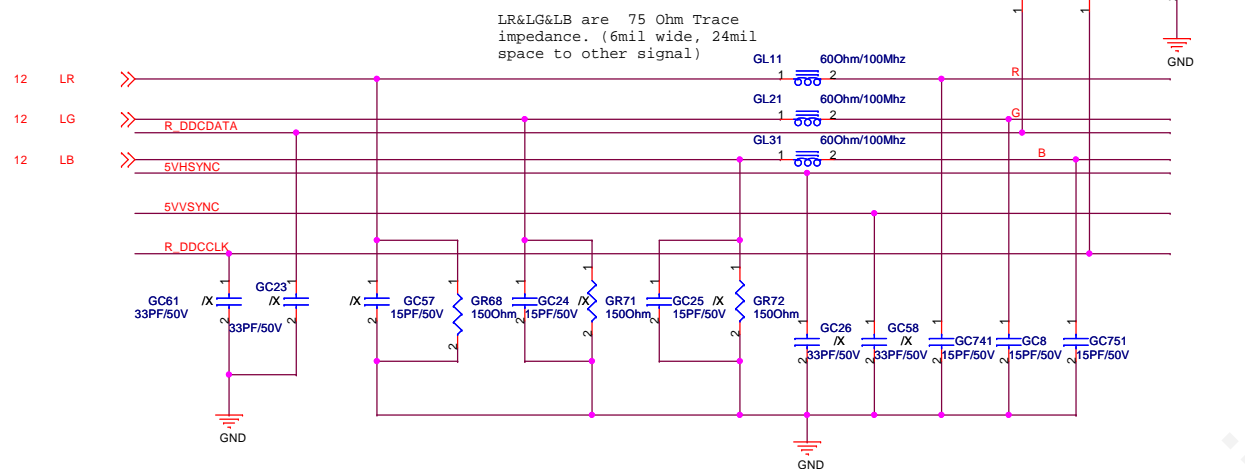


Parallel Port



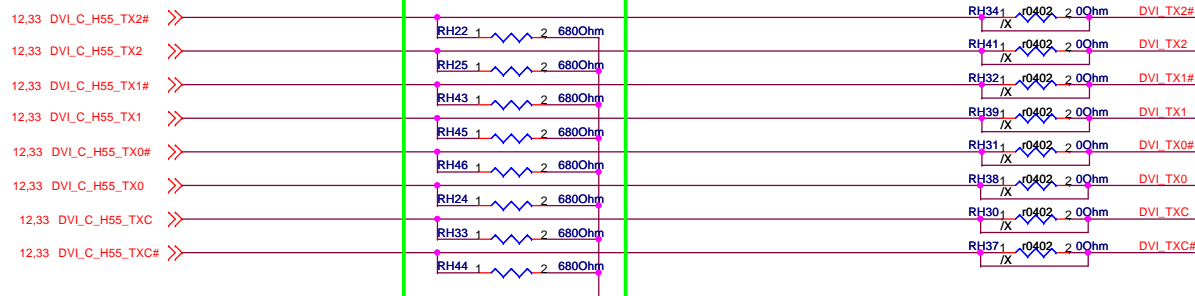
IR





DVI CONNECTOR

BOM爲1%



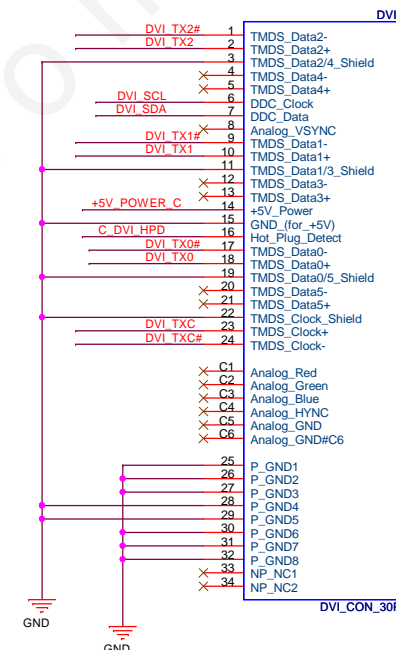
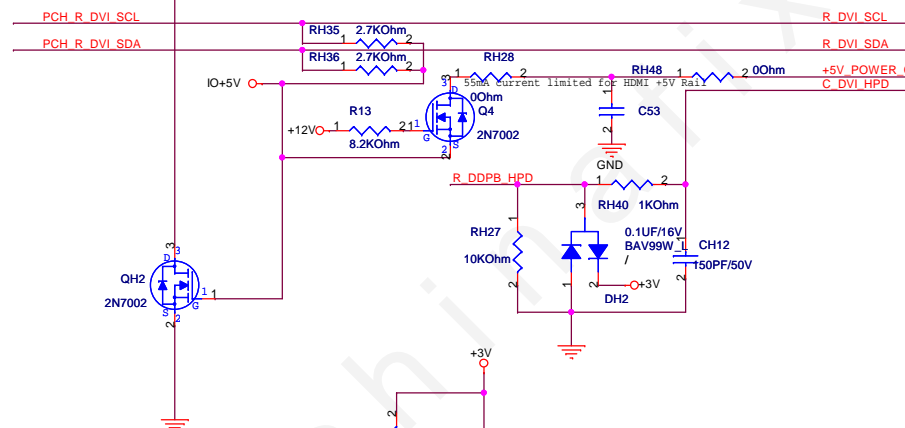
DVI_TX2# 12,33
DVI_TX2 12,33

DVI_TX1# 12,33
DVI_TX1 12,33

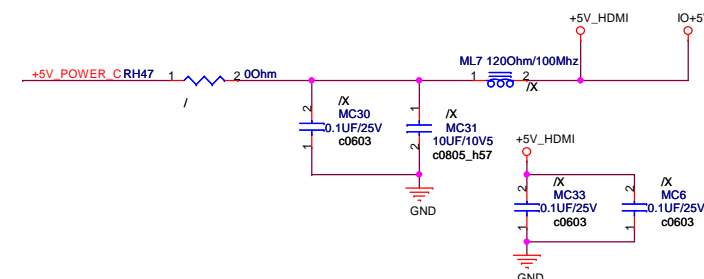
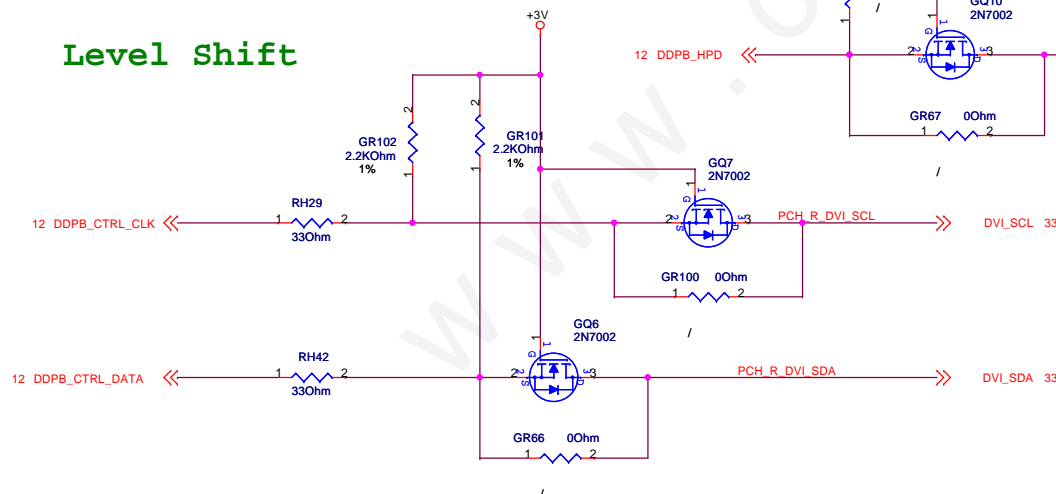
DVI_TX0# 12,33
DVI_TX0 12,33

DVI_TXC 12,33
DVI_TXC# 12,33

C_DVI_HPD 33



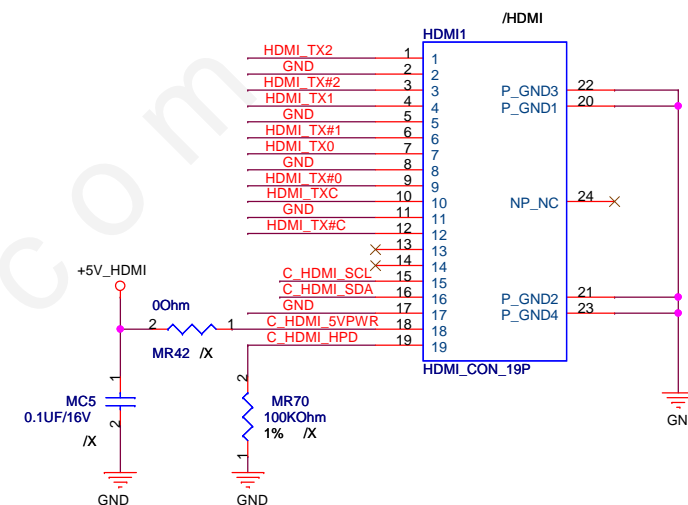
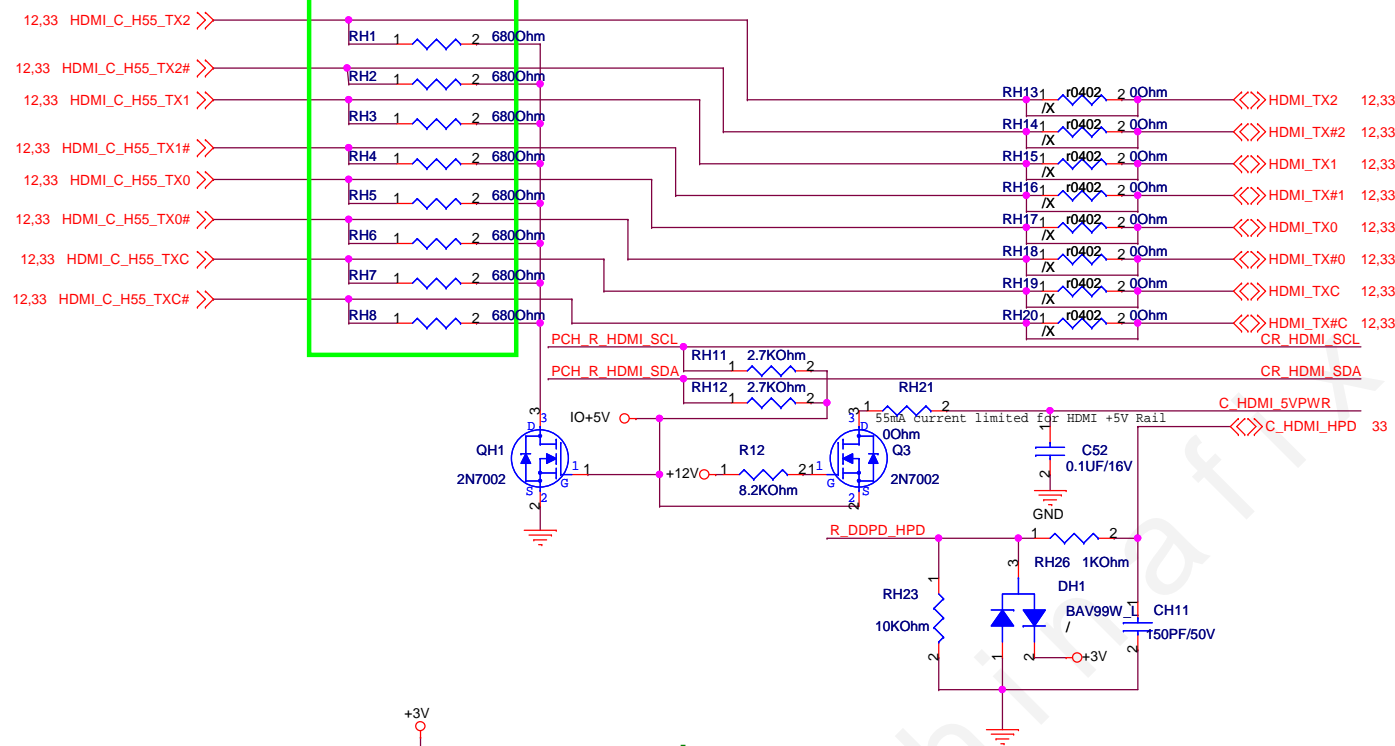
Level Shift



H61MU3S3

HDMI CONNECTOR

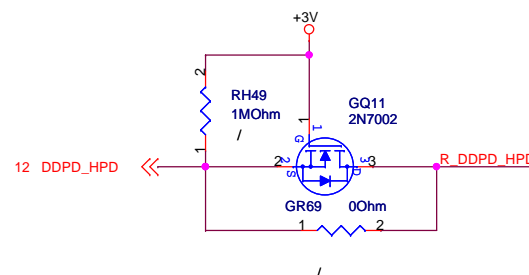
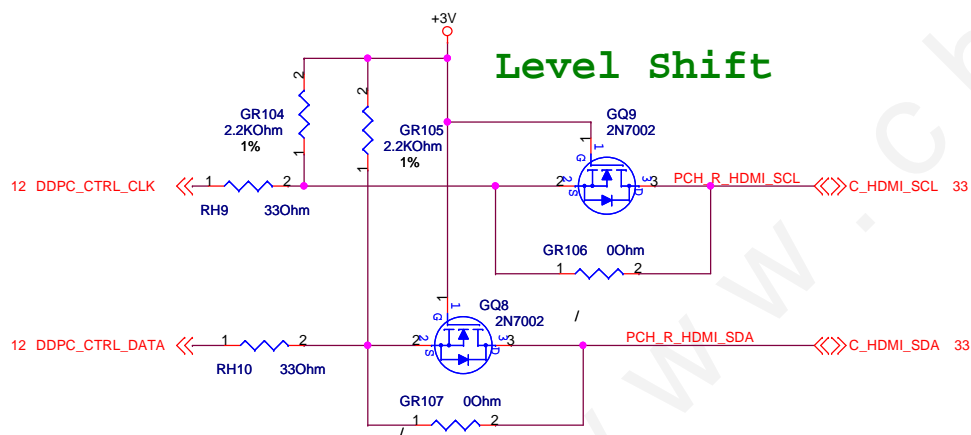
BOM爲1%



33 C_HDMI_SCL >>> C_HDMI_SCL

33 C_HDMI_SDA >>> C_HDMI_SDA

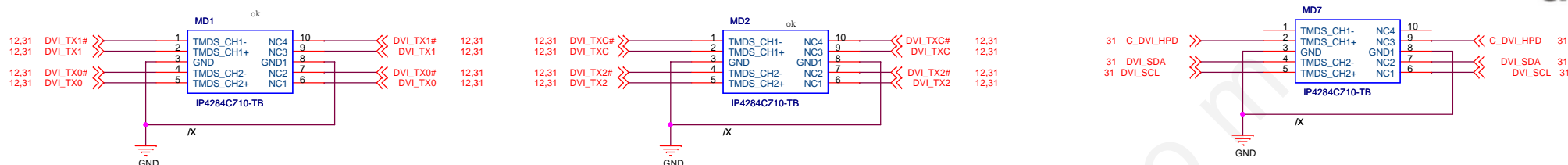
Level Shift



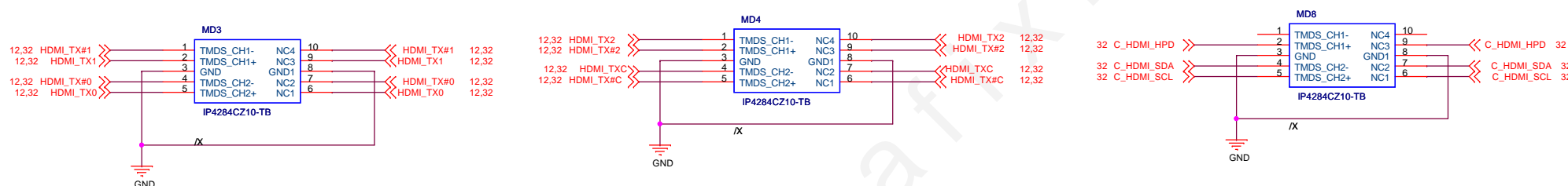
H61M/U3S3

ASRock		Title : HDMI & DVI	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size	Project Name	H61M Pro3	
Custom		Rev 1.02	
Date: Tuesday, December 28, 2010		Sheet	32 of 44

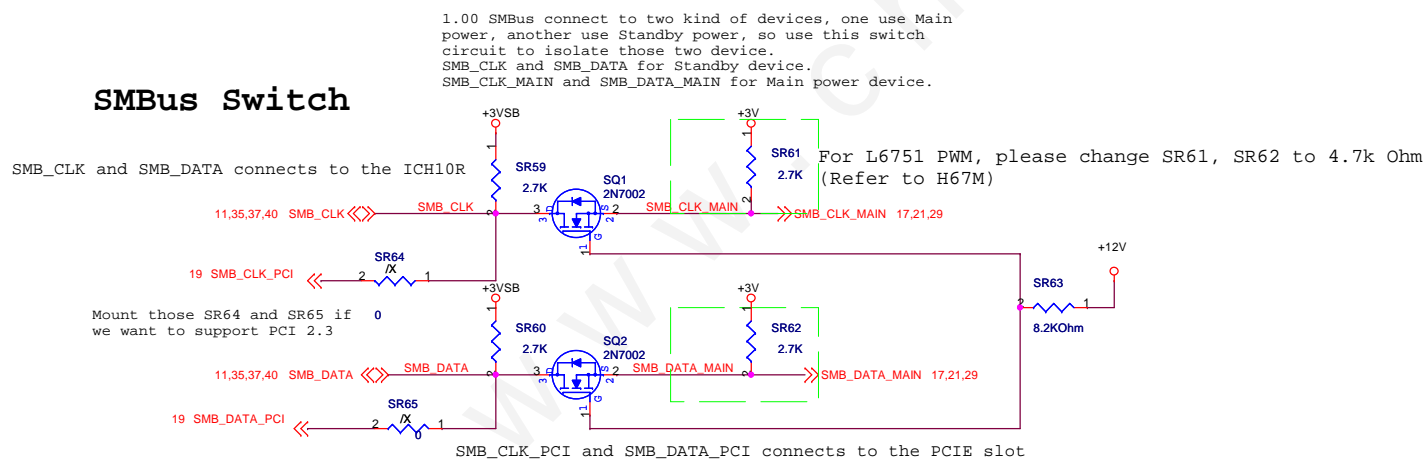
DVI



HDMI

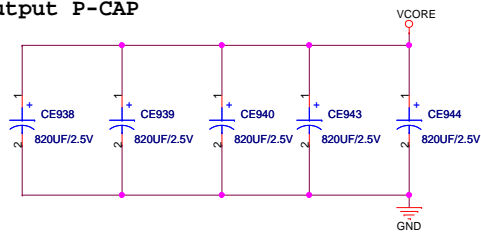


SMBus Switch

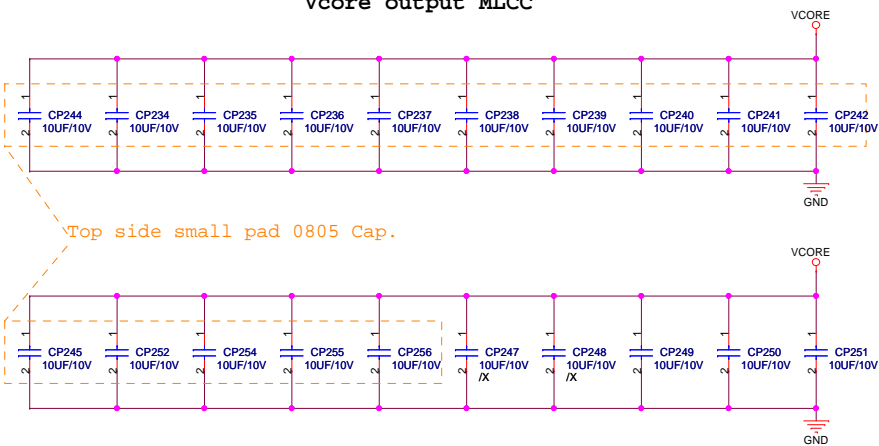


H61MU/3S3

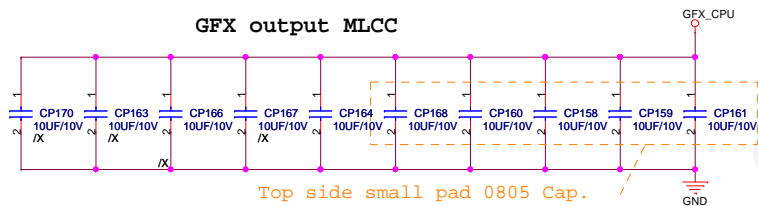
Samwha Cap. Vcore output P-CAP



Vcore output MLCC

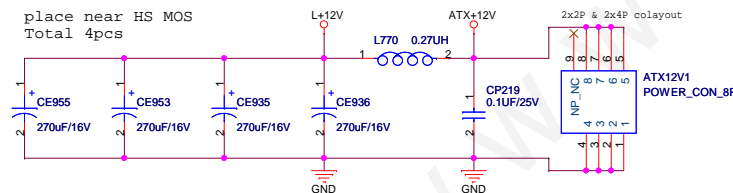


GFX output MLCC



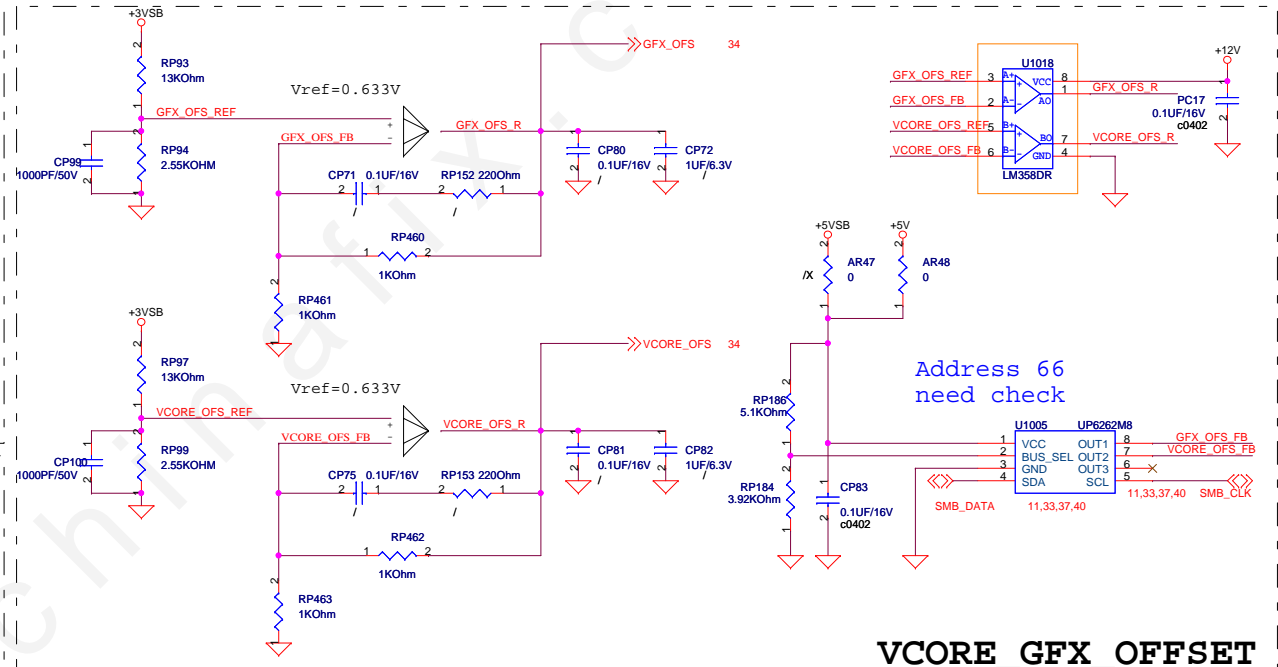
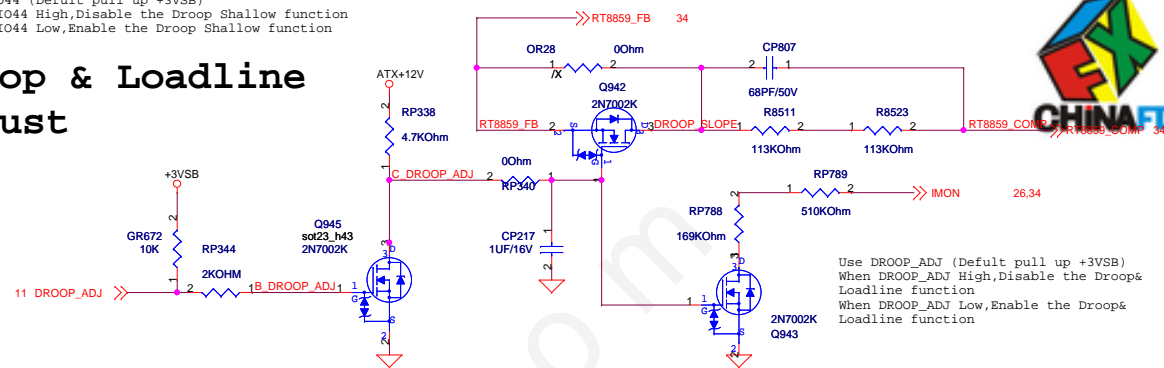
Vcore Input P-CAP

place near HS MOS
Total 4pcs

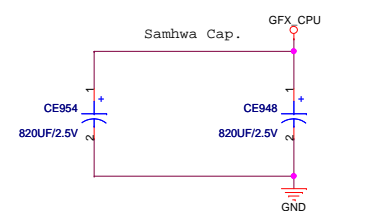


Droop & Loadline Adjust

Use GPIO44 (Default pull up +3VSB)
When GPIO44 High, Disable the Droop Shallow function
When GPIO44 Low, Enable the Droop Shallow function

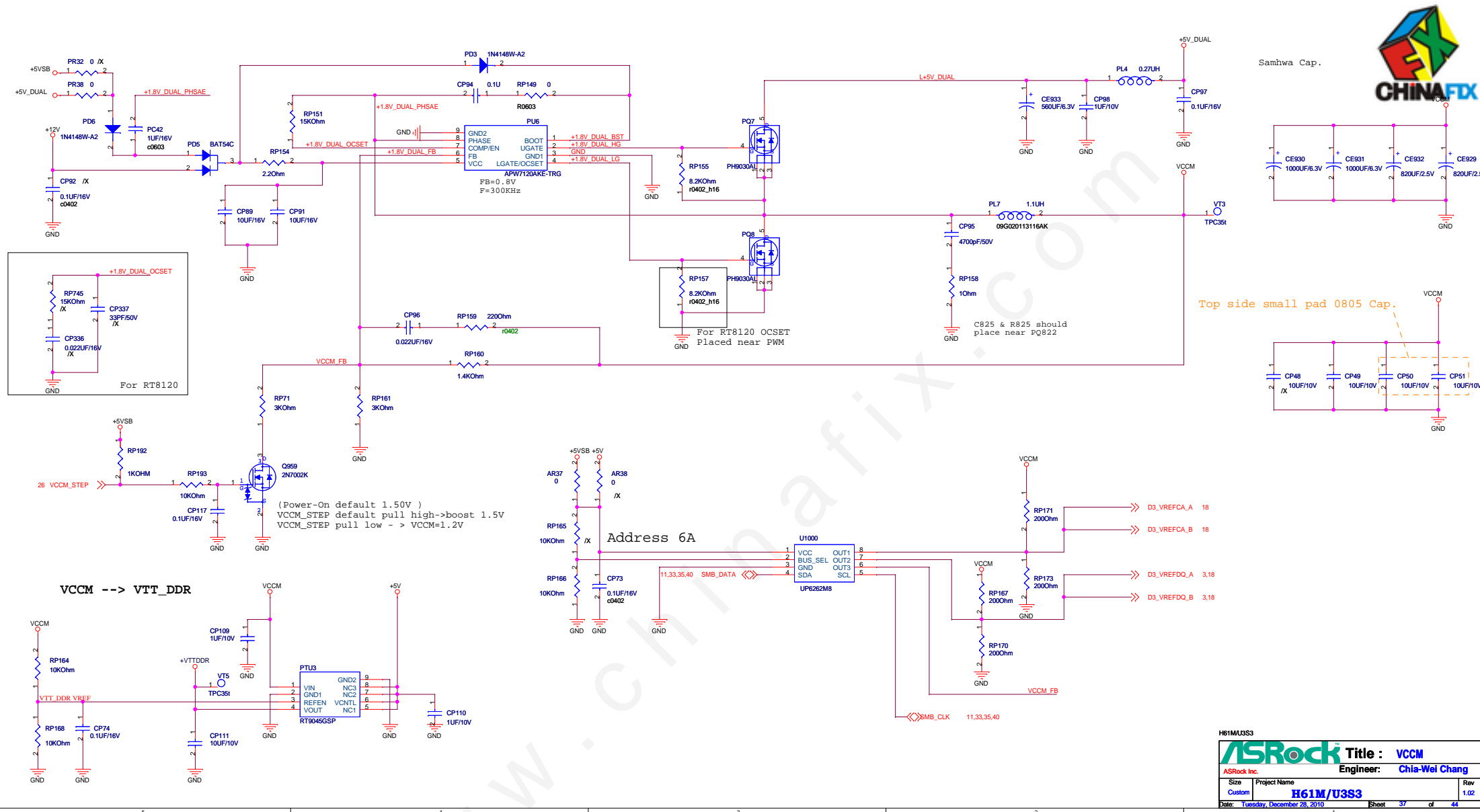



GFX output MLCC



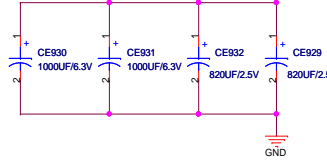
H61M/U3S3

ASRock		Title : CPU CAP & Offset	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size	Project Name	Rev	
Custom	H61M/U3S3	1.02	
Date:	Tuesday, December 28, 2010	Sheet	35 of 44

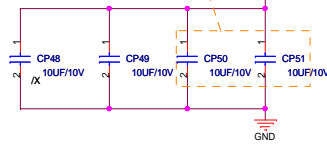




Samhwa Cap.

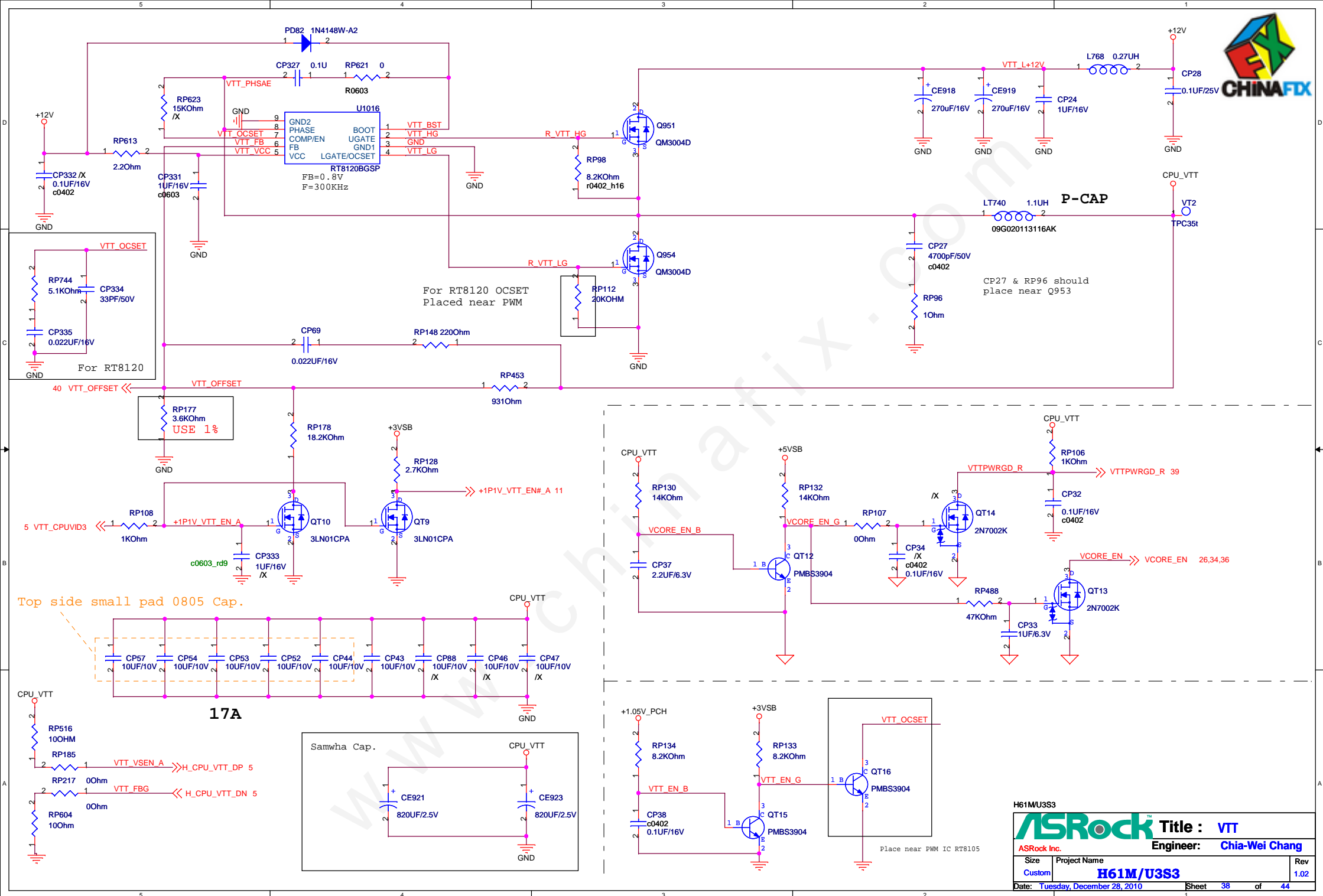


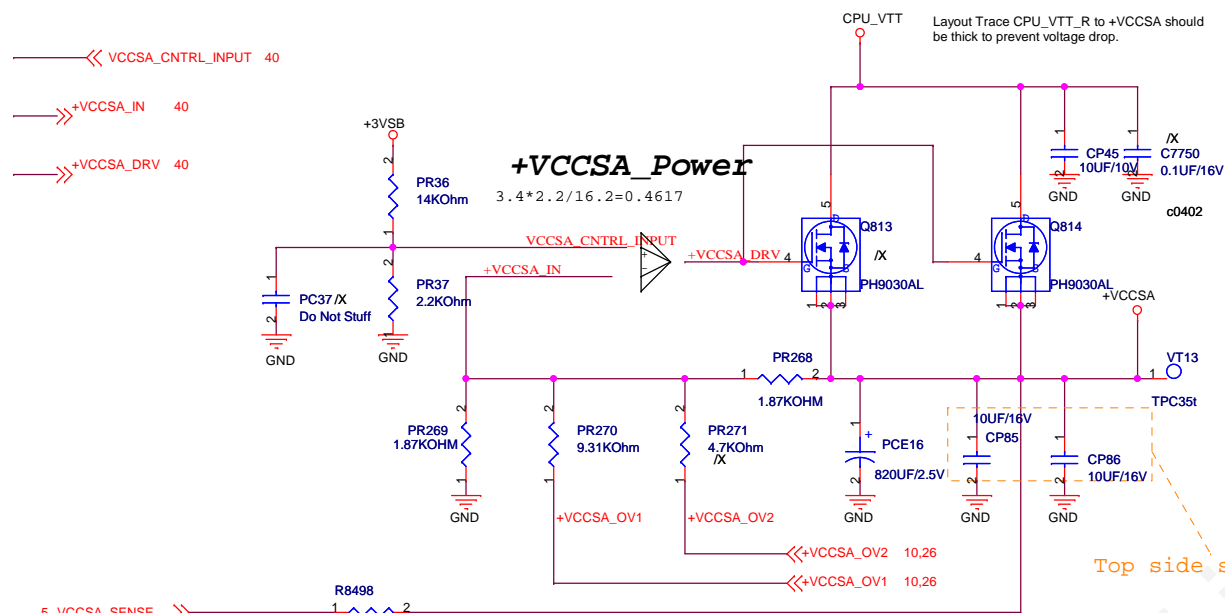
Top side small pad 0805 Cap.



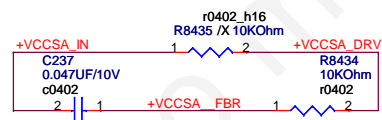
H61MU3S3

ASRock		Title : VCCM	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size	Project Name	Rev	
Custom	H61M/U3S3	1.02	
Date: Tuesday, December 28, 2010	Sheet 37	of	44

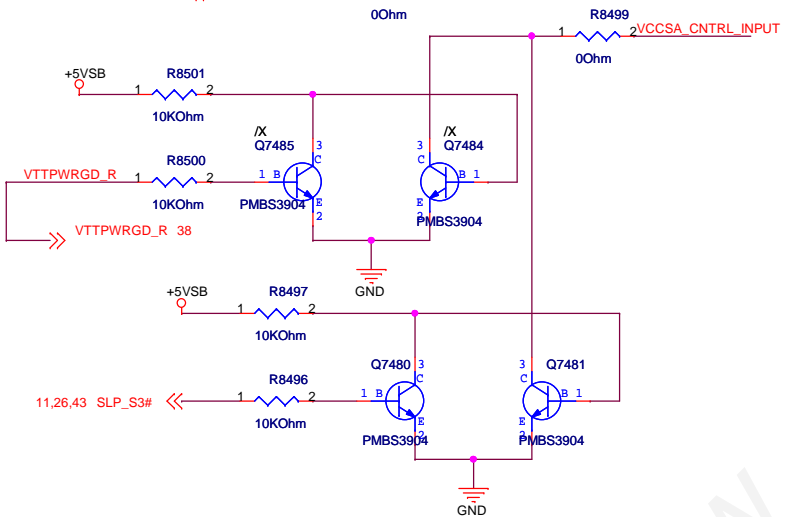




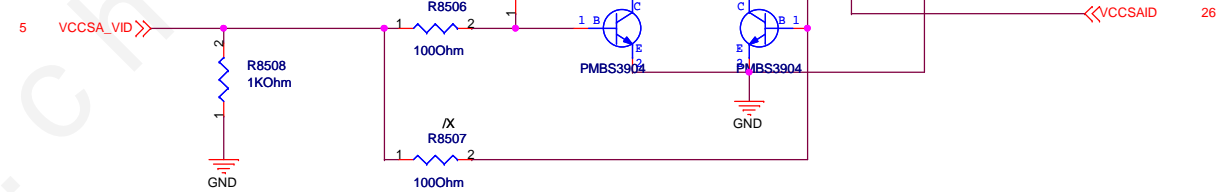
+VCCSA	GPIO17	GPIO16
0.925V	H	H (default)
1.016V	H	L
1.107V	L	H
1.200V	L	L



+VCCSA	OV1	OV2
0.925V	H	H (default)
1.016V	H	L
1.107V	L	H
1.200V	L	L



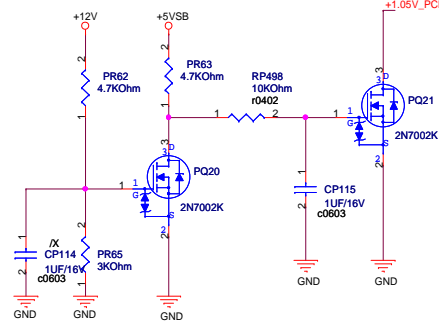
VID=0, VCCSA=0.925V
VID=1, VCCSA=0.85V



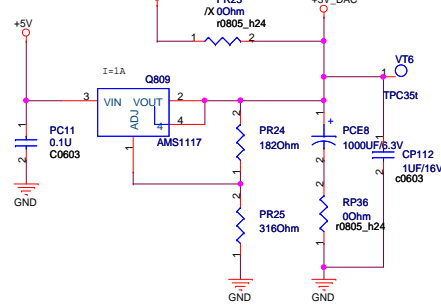
H61MU3S3

ASRock		Title : CPU OV 2V	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size B	Project Name H61M/U3S3		Rev 1.02
Date: Thursday, January 20, 2011		Sheet 39 of 44	

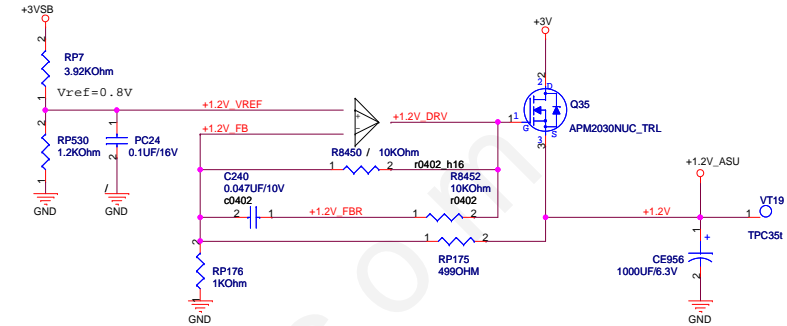
Soft Start - PCH



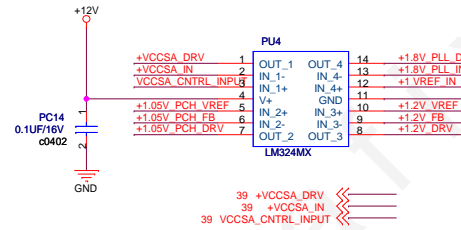
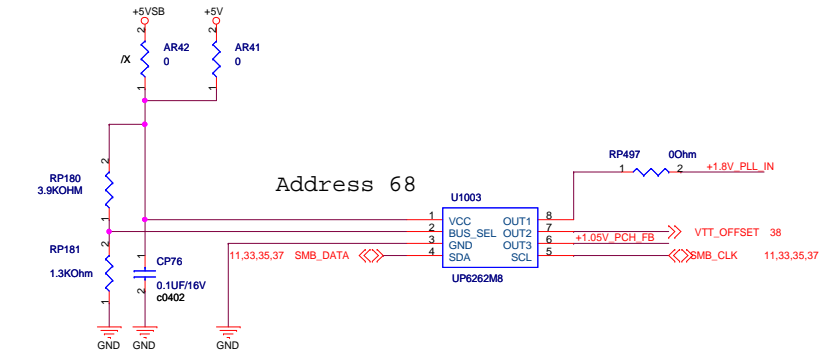
+3.3V_DAC



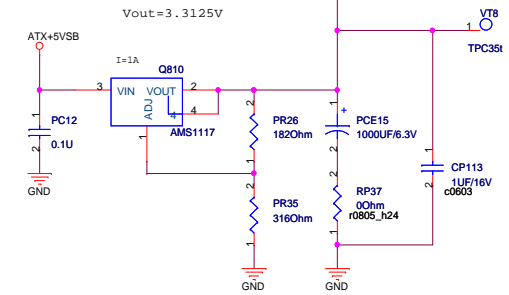
+1.2V Power



Address 68

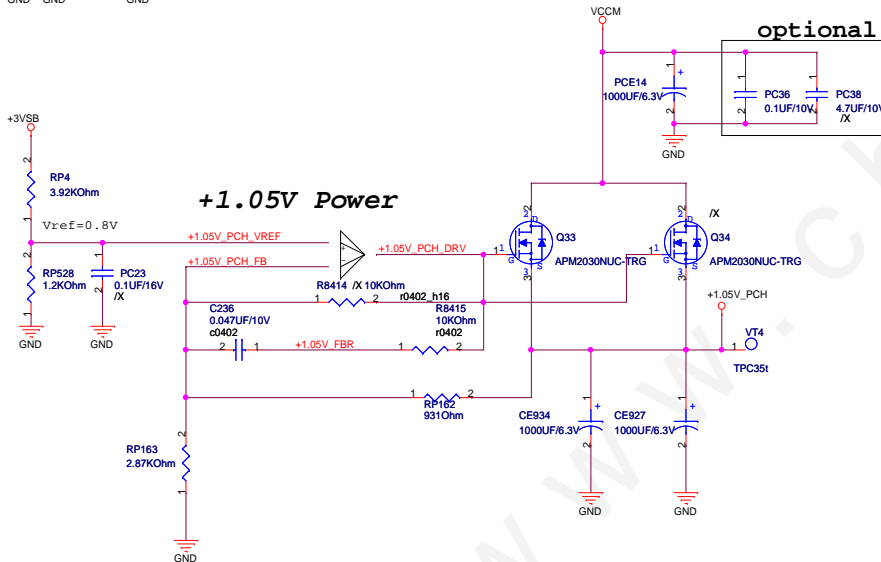


+3VSB_A

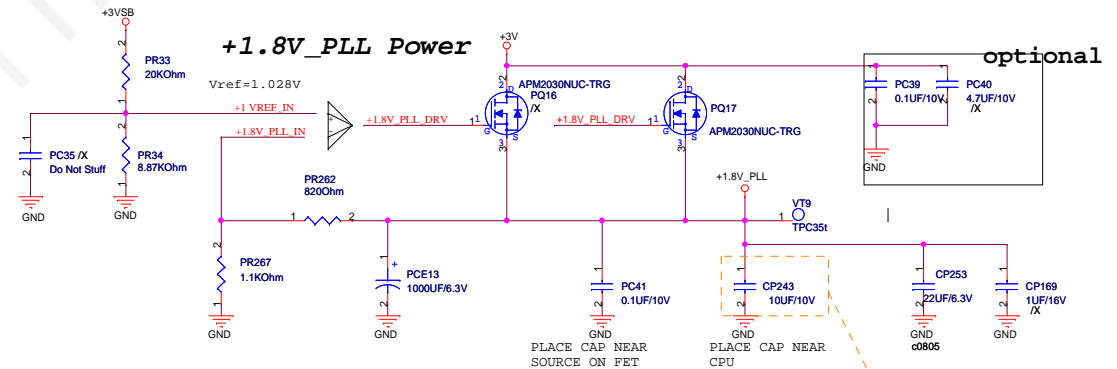


optional

+1.05V Power



+1.8V_PLL Power

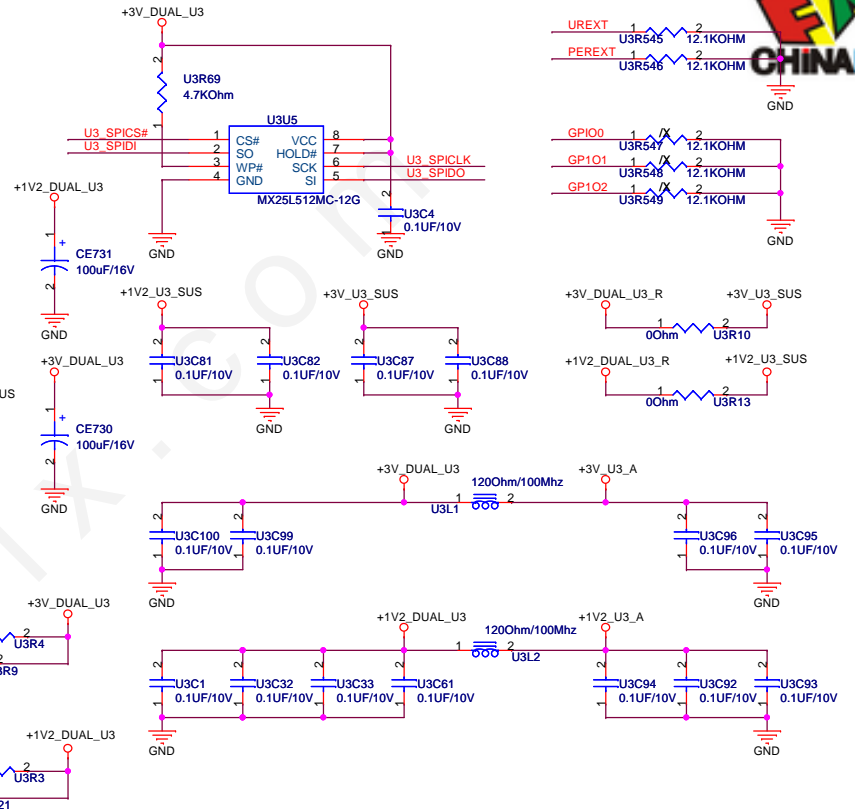
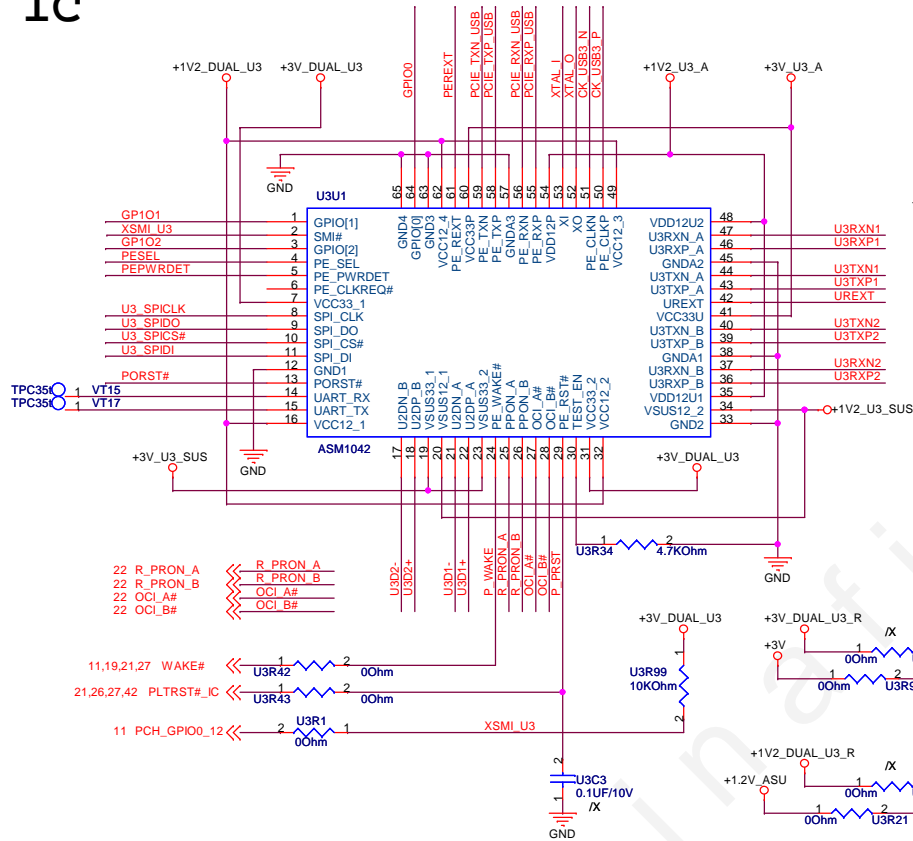
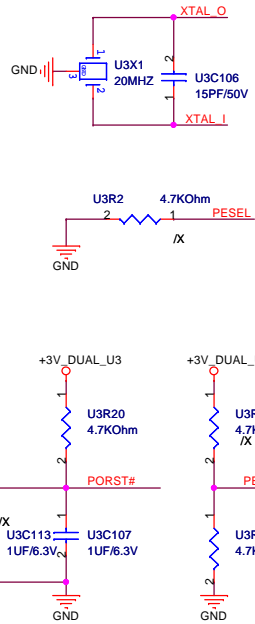


Top side small pad 0805 Cap.

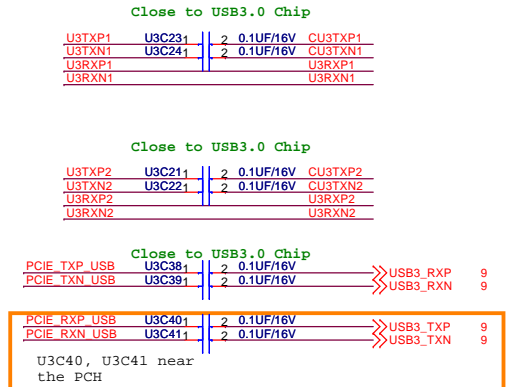
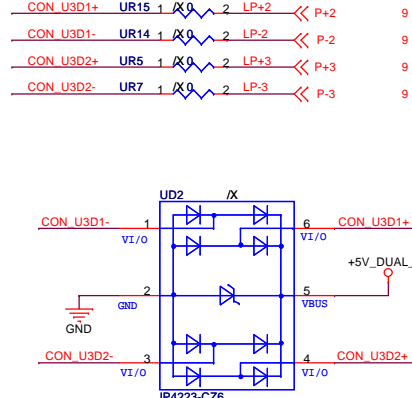
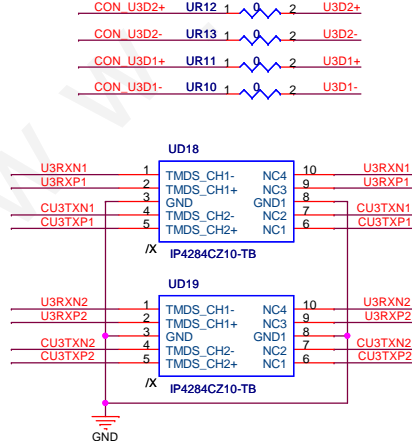
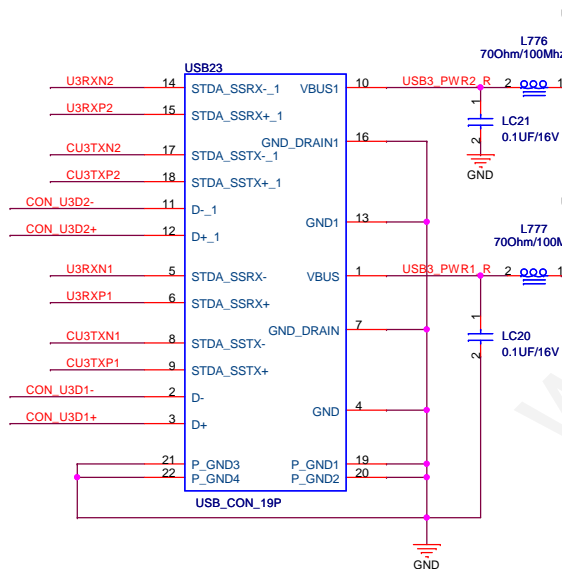
H61M/U3S3

ASRock		Title : CPU OV 2V	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size	Project Name	Rev	
Custom	H61M/U3S3	1.02	
Date: Monday, January 03, 2011	Sheet 40	of 44	

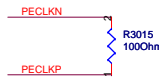
ASM1042 USB3 IC



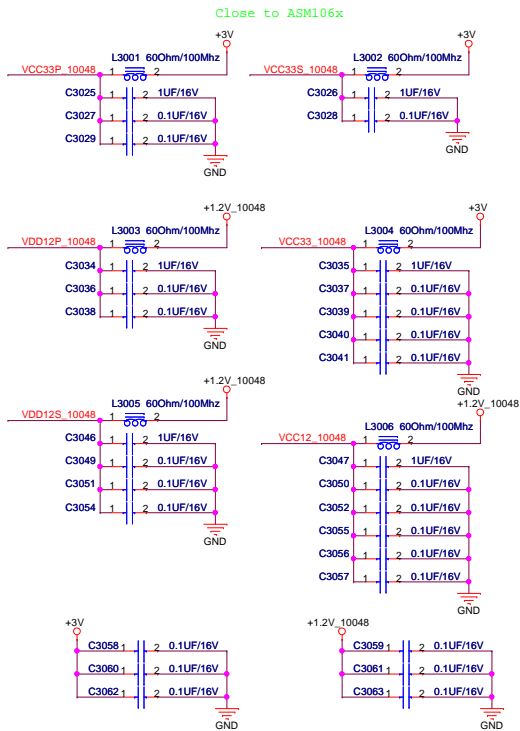
USB3 Con.



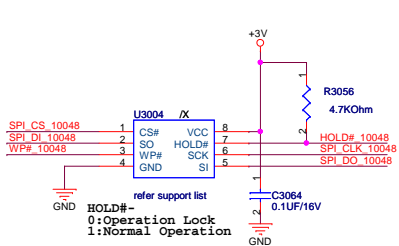
For EMI



Close to ASM106x

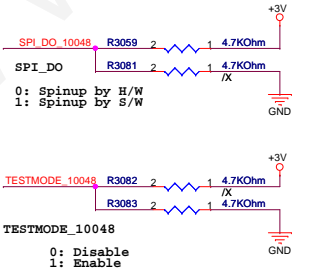


SPI ROM

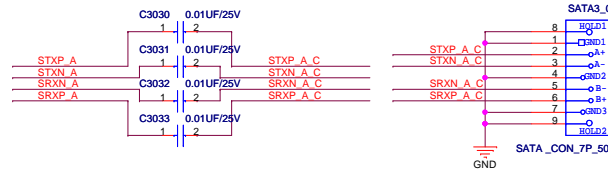


For Testing:
Lock ROM data
on the testing
machine to
prevent the ROM
data being
destroyed.

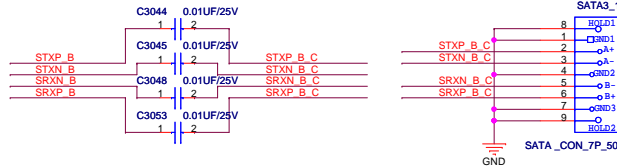
H/W Strapping



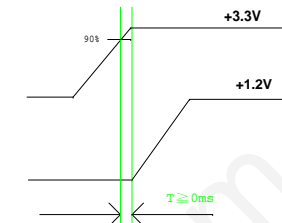
SATA PORT A



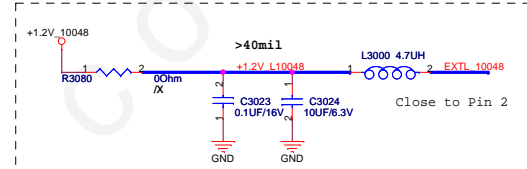
SATA PORT B



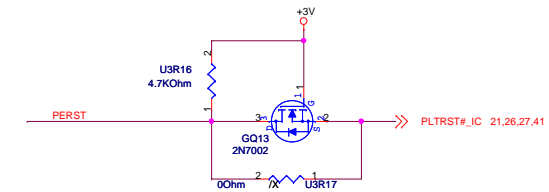
Power up sequence



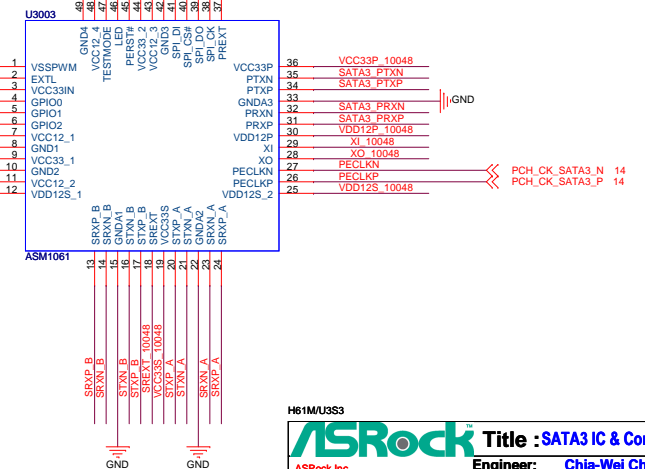
XI & XO follow differential layout rule for Min. jitter



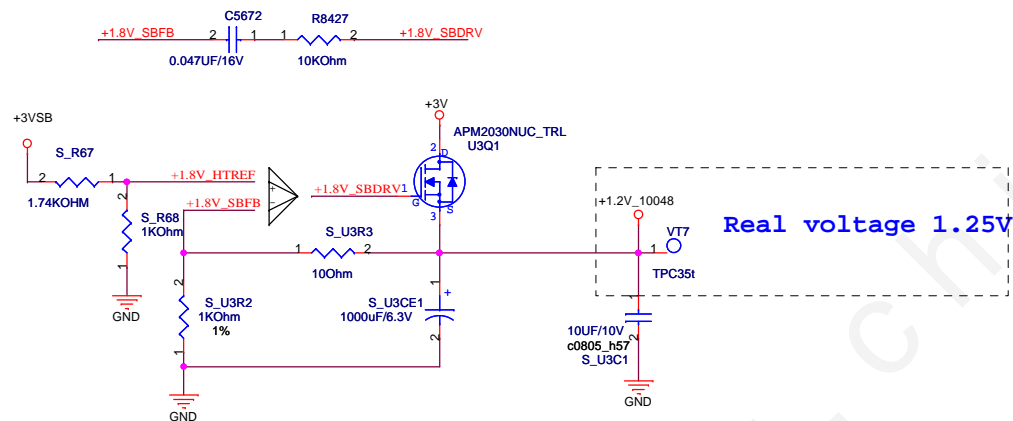
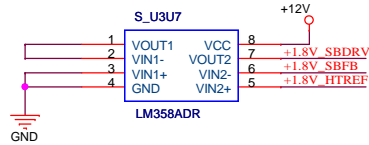
Reserve internal 1.2V voltage



LED_10048 >>> LED_10048 20

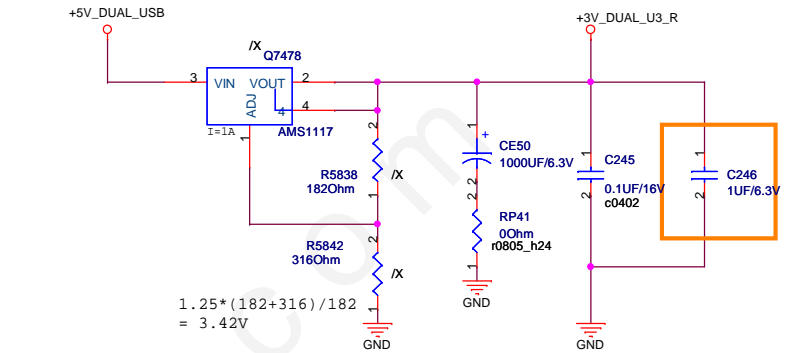


SATA3 Power

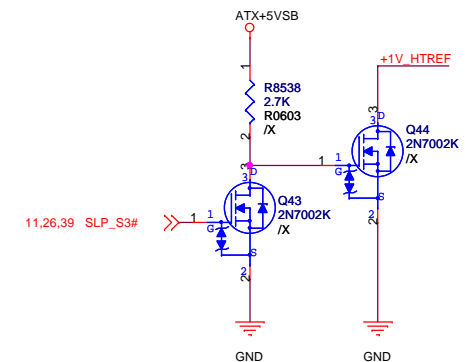
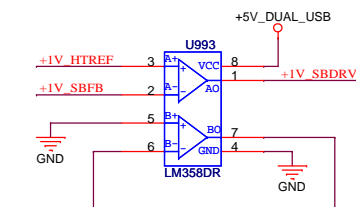
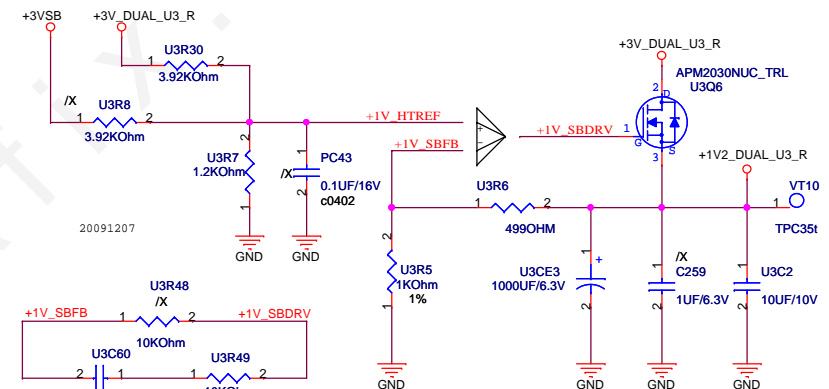


Real voltage 1.25V

Asmedia USB3 Power



$$1.25 * (182 + 316) / 182 = 3.42V$$



H61M/U3S3

ASRock Inc.		Title : SATA3 & USB3 PWR	
Engineer: Chia-Wei Chang		Rev 1.02	
Size Custom	Project Name	H61M/U3S3	
Date: Tuesday, December 28, 2010	Sheet 43	of 44	

SCREW_HOLE

